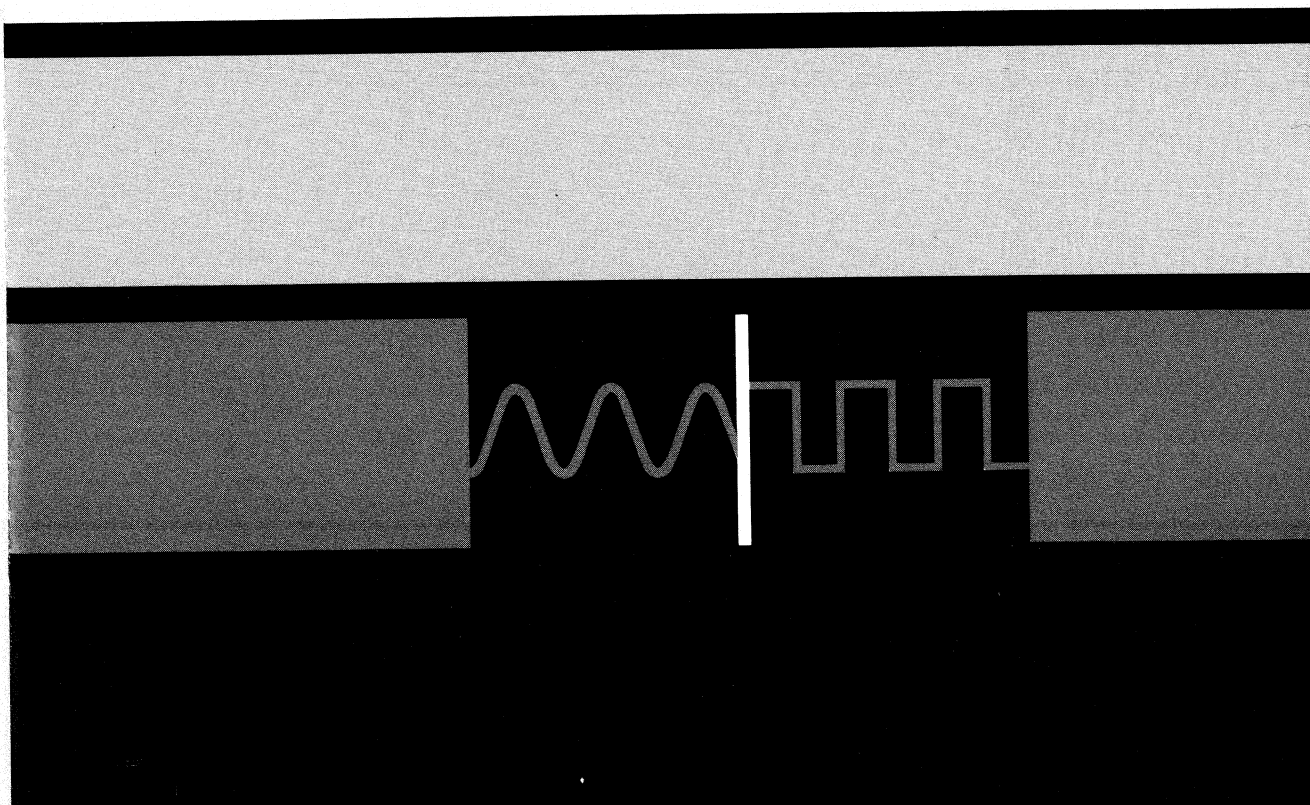
Siliconix

Telecommunications Data Book

November 1979



Siliconix

REVISED TELECOMMUNICATIONS DATABOOK, NOVEMBER 1979

Contents

UPDATE

DF331A AND DF332A ARE IMPROVED VERSIONS OF THE DF331 AND DF332. THE IMPROVEMENTS MADE THE LOGIC INPUTS QUASI-TTL COMPATIBLE AND IMPROVED SIGNAL TO DISTORTION AND GAIN TRACKING PERFORMANCE. THE A VERSIONS ARE *DIRECT REPLACEMENTS* FOR THE ORIGINAL PARTS. THE DF334 AND DF334A ARE IDENTICAL SINCE IT WAS INTRODUCED WITH THE IMPROVEMENTS.

Siliconix

Introduction to Telecommunications Circuits

Siliconix is a high technology manufacturer of sophisticated integrated circuits for the telecommunications industry. The devices and applications data in this catalog are intended to provide designers with state of the art information on proven telecommunications circuits.

The circuits in this catalog although characterized for usage by the telecommunications industry also have application in non-telecommunication areas. The DF331A, DF332A PCM CODEC, for example, is ideally suited for microprocessor interface and control applications.

Siliconix

Product Selector Guide

APPLICATION	DESCRIPTION	PRODUCT
1) Replacing Conventional Rotary Dial Phones with Push Button Keyboards	**Loop Disconnect Dialer**	
	Double Contact Keyboard	DF320/DF321/DF322
2) Converting and Compressing Voice Signal into Digital PCM Format 3) General Usage Companding A/D, D/A Converters with Serial Digital Format	**CODEC Companding A/D-D/A Converter Set**	
	μ-255-Law	DF331A/DF332A/DF334A
	A-Law	DF341/DF342

Siliconix

Telecommunications Data Book

Printed in U.S.A.

Siliconix incorporated reserves the right to make changes in the circuitry or specifications in this book at any time without notice.

Siliconix incorporated assumes no responsibility for the use of any circuits described herein and makes no representations that they are free from patent infringement.

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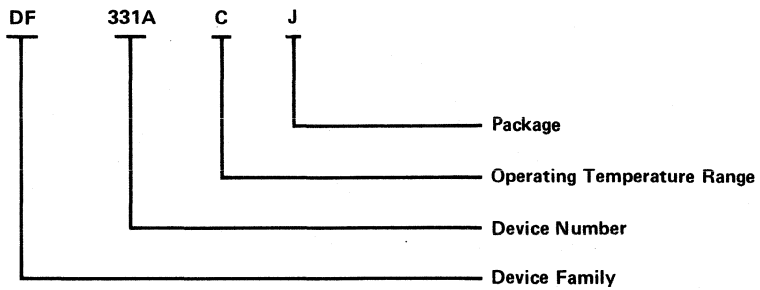
Device Ordering Information



DEVICE FAMILY
(2 Letters)

DF – Digital LSI Function

DEVICE NUMBER
(3-Digit or 3-Digit and 1 Letter Designation)

OPERATING TEMPERATURE RANGE
(1 Letter)

C – 0 to 70°C

D – –40 to 85°C(Applies to Telecommunication Products Only)

C and D temperature range parts receive commercial processing.

All possible combinations of device types, temperature ranges and package types are not necessarily available. Consult individual data book pages for complete information.

PACKAGE
(1 Letter)

J – Dual In-Line Package – Plastic

P – Dual In-Line Package – Side Braze

R – Dual In-Line Package – Side Braze

Siliconix

Product Information

FET Analog Switches

Siliconix's JFET, MOSFET and Integrated Circuit technology has been utilized to produce an extensive family of Analog Switches. These Integrated Circuits are used in many high-reliability military and aerospace applications such as the Mercury, Gemini, Apollo and Skylab manned space programs.

Since 1968, monolithic multi-channel switches with integrated drivers have been part of the Siliconix Analog Switch family.

Subsequently, high performance JFET switches packaged with Integrated Circuit drivers offering low ON resistance, high OFF isolation, fast switching speed and excellent frequency response were added. (DG181 series).

Following this family came the DG506 series, CMOS switches and multiplexers up to 16 channels.

The most recent addition is the DG300 series; these switches combine very low power supply current with high speed and form a low cost alternate for the DG181 series.

LSI/LINEAR

Siliconix is an industry leader in A/D Conversion, **Telecommunications Circuits**, Micropower Linear, Smoke Detector Circuits, Interface and Timing Products. Products ranging from sophisticated instrumentation to consumer smoke detectors incorporate Siliconix linear I.C.'s. Advanced processing capabilities used in the manufacture of these products range from high and low voltage CMOS to bipolar–PMOS. High reliability processing procedures combined with volume production capabilities complement state of the art products.

Field Effect Transistors

Siliconix has maintained technical leadership in P- and N-Channel Junction FETs, and offers the most complete product line in the industry. FETs are characterized for such applications as low-drive d-c amplifiers, low-noise low-frequency amplifiers, high-frequency amplifiers (to 1 GHz), low gate current circuits (10^{-13} A), and analog switching (ON resistance as low as 2.5 Ω).

Both N- and P-Channel MOSFETs are also available, with applications aimed mainly at analog switching.

P-Channel enhancement mode devices are offered with ON resistance ranging from 20 Ω to 1K Ω, and with breakdown voltages as high as 75 V. N-Channel MOSFETs are available in either enhancement or depletion mode structures. Depletion mode devices are also used in amplifiers with very low input currents (r_{DS} 10^{13} Ω)

Most JFETs and MOSFETs are available in chip or wafer form.

High Reliability Devices

Siliconix capability in providing high-reliability devices to meet stringent military or aerospace applications is amply demonstrated by the company's qualification as a supplier for Mercury, Gemini, Apollo and the Viking 75 Mars orbiter/lander. Siliconix has a number of standard Hi-Rel screening options that can be applied to standard products. These options include MIL-STD-883 for microcircuits and MIL-STD-750 for discrete FETs. In addition, Siliconix offers certain JEDEC-registered FETs with JAN, JANTX, and JANTXV processing. If other screening options are required to meet individual customer requirements, Siliconix can provide special additional inspections and controls to meet the most exacting demands.

The company has an in-house Scanning Electron Microscope facility and maintains many on-going product and process evaluation programs for standard products. Siliconix can supply SEM qualified products to meet individual customer requirements.

VMOS Power FETs

Siliconix continues to expand its technological leadership in the field effect transistor product area with the introduction of industry's first power MOSFETs. N-Channel enhancement mode devices are available in a variety of packages (TO-3, TO-39, 380 SOE) and are capable of operating up to 12 Amps and 90V, with ON resistances as low as 0.3 ohms. Typical applications for MOSPOWER transistors include interfacing from logic to electromechanical devices, power outputs in audio amplifiers, high speed switching in power supplies and amplifiers, broadband RF amplifiers up to 200 MHz, and high speed data transmission circuits.

Telecommunications

Data Sheets
Application Note
Design Aids
Technical Articles

Index 1

CMOS loop disconnect dialers

Siliconix

designed for . . .

- **Push Button Telephones**
- **Repertory Dialers**
- **Telex**
- **Mobile Telephones**
- **Security and Fire Alert Systems**
- **Emergency Number Dialers**

BENEFITS

- **Eliminates the Need for Regulated Supplies**
  - 2.5 V to 5.5 V V_{DD} Range
- **Minimizes Power Consumption**
  - Standby Dissipation $< 3\ \mu W$
- **Low Cost**
  - Simple Support Circuitry
  - No External Power Up Reset Components
- **Minimizes External Components**
  - On Chip Circuitry for: Keyboard Debouncing; Last Number Repeat; Input Terminations
- **Versatile**
  - Selectable Mark/Space Ratios, Impulsing Speeds, Interdigital Pause
  - Fast Data Entry Possible

DESCRIPTION

The DF320 series of monolithic CMOS Loop Disconnect Diallers each contain all the logic necessary to interface a standard double contact keyboard to a telephone system requiring loop disconnect signalling.

A dial pulsing output and two masking output options are provided to control the impulsing (loop disconnect) and muting functions. The circuit is capable of storing a number string of up to 20 digits and re-dialling this stored number automatically at a later time, initiated by a RE-DIAL input code. Impulsing mark/space ratio (M/S), impulsing rate and interdigital pause (IDP) are all pin programmable to meet most telephone requirements.

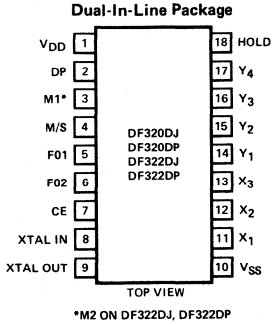
The use of Siliconix low voltage CMOS technology allows operation with an unregulated supply voltage down to a guaranteed minimum of 2.5 V. This feature, together with low operating current, negligible standby current and high noise immunity make the DF320 series easy to interface from long telephone lines.

External component count is minimized by the inclusion of an on-chip clock oscillator, high impedance pull-down terminations to programming inputs as well as pull-up terminations to the keyboard giving direct interfacing.

The Loop Disconnect Dialler is available in three pinout options. The DF320 provides the functions most commonly required in the push button telephone application. M1 is the masking option which remains at logic "1" throughout the dialling sequence. The DF322 is identical to the DF320 except that M2 is offered instead of M1. The M2 masking option is at logic "1" only during impulsing, allowing the telephone line to be monitored during the IDP. The DF321 is a multi-option version which offers both M1 and M2 together with FD, IDP and SYS CK.

PIN CONFIGURATIONS

Dual-In-Line Package

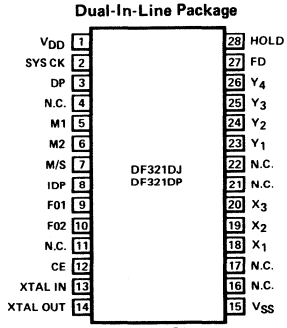


TOP VIEW

*M2 ON DF322DJ, DF322DP

ORDER NUMBERS DF320DJ OR DF322DJ
SEE PACKAGE 19
ORDER NUMBERS DF320DP OR DF322DP
SEE PACKAGE 20

Dual-In-Line Package



TOP VIEW

ORDER NUMBER DF321DJ
SEE PACKAGE 14
ORDER NUMBER DF321DR
SEE PACKAGE 13

ABSOLUTE MAXIMUM RATINGS

$V_{DD} - V_{SS}$ . . . . . −0.3 V to 8 V
Voltage on Any Pin . . . . . V_{SS} − 0.3 V to V_{DD} + 0.3 V
Current at Any Pin . . . . . 10 mA
Operating Temperature. . . . . −40 to +85°C
Storage Temperature (P Package) . . . . . −65 to +150°C
(J Package). . . . . −65 to +125°C
Power Dissipation (P Package)* . . . . . 1000 mW
(J Package)** . . . . . 450 mW

*Derate 16 mW/°C above 75°C. All leads soldered to PC board.
**Derate 6.3 mW/°C above 25°C. All leads soldered to PC board.

Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits.

ELECTRICAL CHARACTERISTICS

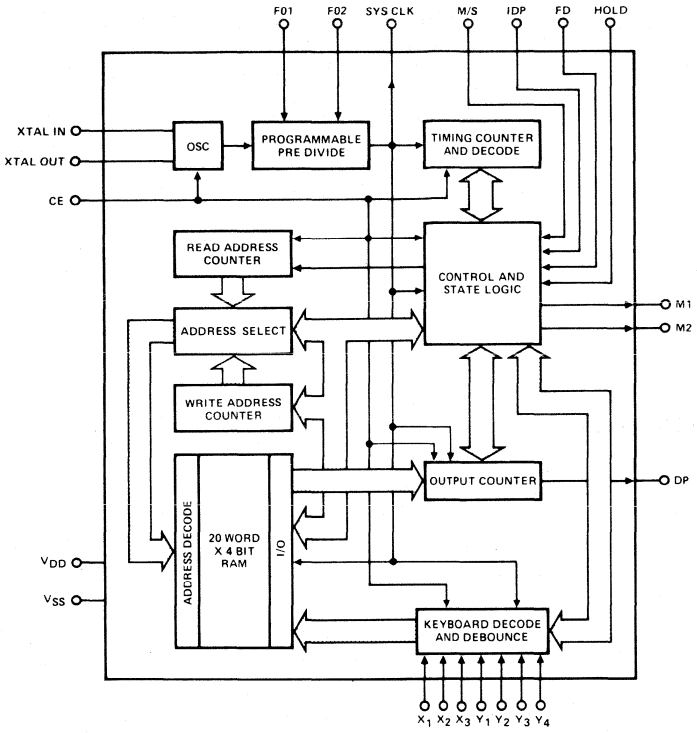
All voltages referenced to V_{SS} unless otherwise noted.

		Characteristic		Min	Typ*	Max	Units	Test Conditions Unless Noted V_{DD} = 3.0 V, T_A = 25°C, f_{CLK} = 3.57945 MHz, See Note 1
1	SUP	V_{DD} Supply Voltage Operating Range		2.5		5.5	V	
2	SUP	I_{DSS} Standby Supply Current			1.0	10.0	μA	CE = V_{SS}
3	SUP	I_{DD} Operating Supply Current			180	250	μA	3.579545 MHz Crystal, $C_{XTALOUT}$ = 12 pF
4	INPUT	I_{IL} Pull-Up Transistor Source Current		−0.5	−3.0	−8.0	μA	$V_{IN} = V_{SS}$ — $X_1, X_2, X_3,$
5	INPUT	I_{IH} Input Leakage Current			0.1		nA	$V_{IN} = V_{DD}$ — Y_1, Y_2, Y_3, Y_4
6	INPUT	I_{IL} Input Leakage Current			−0.1		nA	$V_{IN} = V_{SS}$ — M/S, IDP, F01,
7	INPUT	I_{IH} Pull-Down Transistor Sink Current		0.5	3.0	8.0	μA	$V_{IN} = V_{DD}$ — F02, FD, Hold
8	OUT	V_{OL} Voltage Levels	Low Level		0	0.01	V	No Load — DP, M1, M2
9	OUT	V_{OH} Voltage Levels	High Level	2.99	3		V	No Load — DP, M1, M2
10	OUT	I_{OL} Drive Current	N-Channel Sink	0.8	2.0		mA	V_{OUT} = 2.3 V — DP, M1, M2
11	OUT	I_{OH} Drive Current	P-Channel Source	−0.8	−1.5		mA	V_{OUT} = 0.7 V — DP, M1, M2
12		t_r Output Rise Time			1.0		μs	DP, M1, M2, C_L = 50 pF
13		t_f Output Fall Time			1.0		μs	DP, M1, M2, C_L = 50 pF
14		f_{CLK} Maximum Clock Frequency		3.58			MHz	3.579545 MHz Crystal
15	DYNAMIC	M/S Mark to Space Ratio			2:1			Note 2
16	DYNAMIC	M/S Mark to Space Ratio			3:2			Note 2
17	DYNAMIC	IDP Interdigital Pause			4T		ms	T = Selected Impulsing Period. Note 2
18	DYNAMIC	IDP Interdigital Pause			8T		ms	T = Selected Impulsing Period. Note 2
19	DYNAMIC	Impulsing Rate = 1/T			10		Hz	Note 2
20	DYNAMIC	Impulsing Rate = 1/T			16		Hz	Note 2
21	DYNAMIC	Impulsing Rate = 1/T			20		Hz	Note 2
22	DYNAMIC	Impulsing Rate = 1/T			932		Hz	Note 2
23		t_{ON} Clock Start Up Time			1.5	4	ms	Timed from CE = Logic "1"
24		C_{IN} Input Capacitance			5.0		pF	Any Input

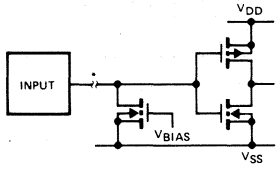
*Typical parametric values are for Design Aid Only, not guaranteed and not subject to production testing. Timing waveforms are subject to production functional test.

NOTES:
1. Logic levels are defined as "0", $V_{IN} < 0.8$ V, "1", $V_{IN} > V_{DD} - 1$ V.
2. See Pin Function, Table 1.

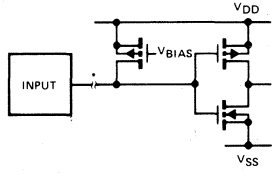
FUNCTIONAL BLOCK DIAGRAM



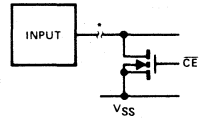
INPUT OUTPUT SCHEMATICS



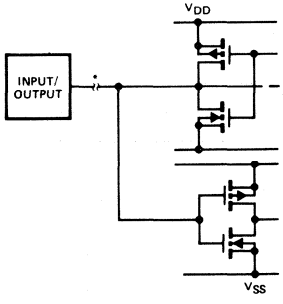
M/S, IDP, F01, F02, FD, HOLD
Figure 1



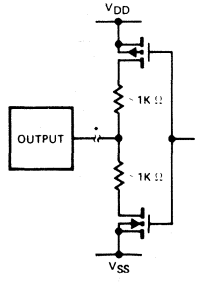
$X_1, X_2, X_3, Y_1, Y_2, Y_3, Y_4$
Figure 2



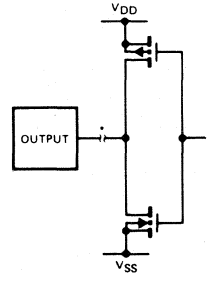
XTAL IN
Figure 3



CE, SYS CLK
Figure 4



DP, M1, M2
Figure 5

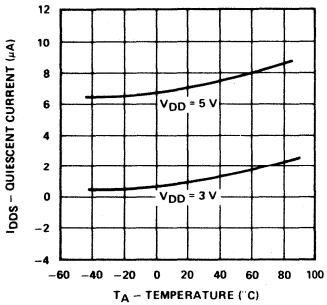


XTAL OUT
Figure 6

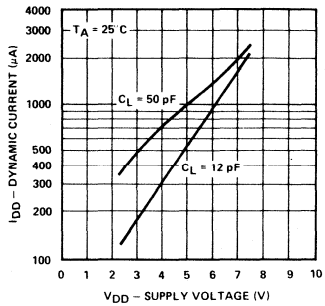
*Circuit Protection Not Shown

TYPICAL CHARACTERISTICS

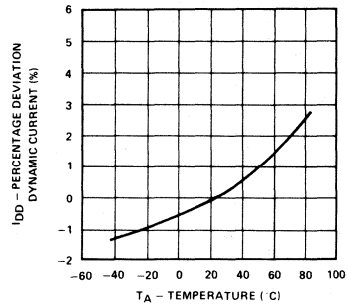
Typical Quiescent Current vs Temperature



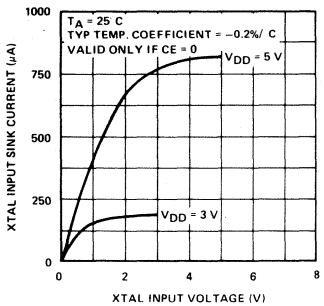
Typical Dynamic Current vs Supply Voltage (V_{DD})



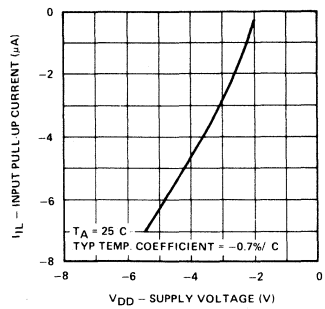
Typical Percentage Deviation of Dynamic Current vs Temperature (Normalized to 25°C)



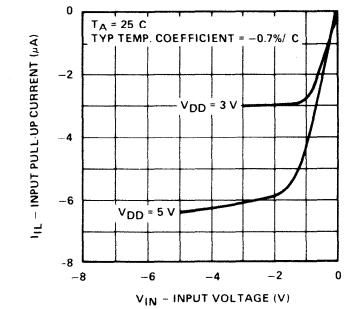
Typical XTAL IN Input Clamp Characteristics



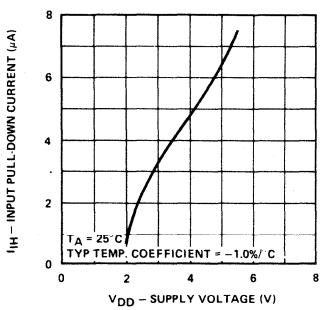
Typical Input Pull-Up Current vs Supply Voltage (X_1, X_2, X_3, Y_1, Y_2, Y_3, Y_4)



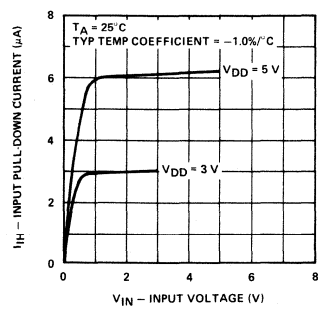
Typical Input Pull-Up Characteristics



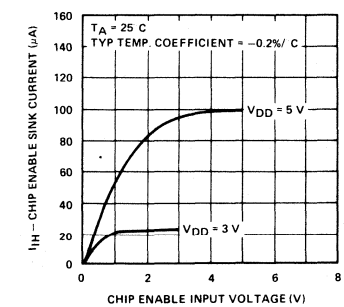
Typical Input Pull-Down Current vs Supply Voltage (M/S, IDP, F01, F02, FD, HOLD)



Typical Input Pull-Down Characteristics

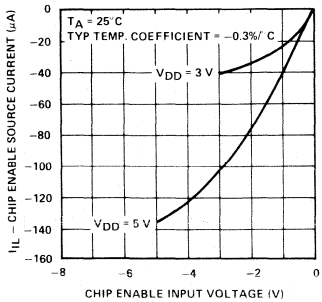


Typical Chip Enable Sink Characteristics

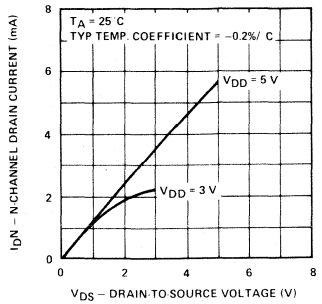


TYPICAL CHARACTERISTICS (Cont'd)

Typical Chip Enable Source Characteristics



Typical Output N-Channel Drain Characteristics (DP, M1, M2)



Typical Output P-Channel Drain Characteristics (DP, M1, M2)

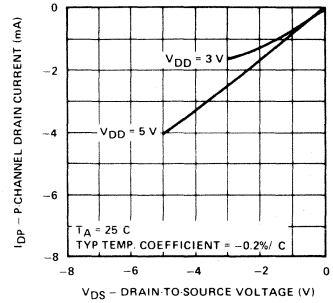


Table 1

PIN FUNCTION	DESCRIPTION
V_{DD}	Positive voltage supply
SYS CLK	Frequency = 30 x Impulsing Rate
DP	Dial Pulsing Output Buffer
M1	Mask 1 (Buffered Output) = Logic "1" during Dialling Sequence
M2	Mask 2 (Buffered Output) = Logic "1" during an Impulse
M/S	Mark/Space (Break/Make) Ratio select. On-chip active pull-down to V_{SS}. O/C: 2:1 V_{DD}: 3:2 Note: O/C = Open circuit, see Figure 7.
IDP	Interdigital Pause. On-chip active pull-down to V_{SS}. O/C: IDP = 8 x Impulsing period V_{DD}: IDP = 4 x Impulsing period See Figures 7 and 8
F01, F02	Impulsing Rate Selection. On-chip active pull-down to V_{SS}.

F01	F02	Nominal Impulsing Rate	Actual* Impulsing Rate	System Clock Frequency
O/C	O/C	10 Hz	10.13 Hz	303.9 Hz
O/C	V_{DD}	20 Hz	19.42 Hz	582.6 Hz
V_{DD}	O/C	932 Hz	932.17 Hz	27,965.1 Hz
V_{DD}	V_{DD}	16 Hz	15.54 Hz	466.1 Hz

*Assumes f_{CLK} = 3.579545 MHz

CE	Chip Enable. Input/Output, left open it is internally controlled by keyboard decode logic. Can be externally forced for manually enabling chip.
XTAL IN	Crystal Input. Active, clamped low if CE = "0", high impedance if CE = "1".
XTAL OUT	Crystal Output. Buffer to drive crystal. Capacitive load on-chip.
V_{SS}	System ground
X_1, X_2, X_3	Column keyboard inputs having active pull-ups to V_{DD}. Active LOW.
Y_1, Y_2, Y_3, Y_4	Row keyboard inputs having active pull-ups to V_{DD}. Active LOW
FD	Fast Data control. Inhibits debounce circuit to allow fast data entry from repertory dialler memory or other electronic input. On-chip active pull-down to V_{SS}. O/C: Normal Operation V_{DD}: Inhibit Debounce circuit
HOLD	Prevents further impulsing. On-chip active pull-down to V_{SS}. O/C: Normal Operation V_{DD}: No impulsing. If activated during impulsing, hold occurs when the current digit is complete.

FUNCTIONAL DESCRIPTION

1.0 Clock Oscillator – The on-chip oscillator amplifier is connected between the XTAL IN and XTAL OUT pins. The oscillator is completed by connecting a 3,579,545 Hz crystal in parallel with a 10M Ω resistor between XTAL IN and XTAL OUT. When CE = "0" an N-channel transistor clamp is activated, disabling oscillator operation. On the transition of CE to logic "1" a fast oscillator turn-on circuit kicks XTAL IN voltage to the amplifier bias point allowing oscillator operation within 4 ms. The basic clock frequency of 3.58 MHz is predivided by a programmable counter to provide the chip system clock. This is available on pin 2 of the DF321 and is usable to synchronize external logic if required.

As an alternative, an LC oscillator can be formed as shown in Figure 15. Selection of f_{CLK} = 38.4 kHz with F01 connected to V_{DD} will give an impulsing rate of 10 Hz.

It is also possible to control the DF320, DF321, DF322 from an external clock applied to XTAL IN.

2.0 Chip Enable, CE – The Chip Enable pin is used to initialize the chip system. CE = "0" forces the chip into the static standby mode. In this mode the clock oscillator if OFF, internal registers are reset with the exception of the WRITE ADDRESS COUNTER and the circuit is ready to receive a new number or re-dial. While CE = "0" data cannot be received by the chip, but data previously entered and stored is maintained. When CE = "1" the clock oscillator is operating, the internal registers are enabled, and data can be entered from the keyboard up to a maximum of 20 digits.

CE is primarily controlled by a logic gate with function

F = KEYBOARD INPUT + M1 + HOLD

where + denotes logical OR.

To operate this gate, a resistor and capacitor should be connected in parallel between CE and V_{SS}. When the chip is used in the CE INTERNAL CONTROL MODE power ON reset occurs when V_{DD} is applied, since a logic "0" appears on the CE pin. The chip remains in the static standby condition until it receives the first keyboard input after V_{DD} is applied. This is decoded and causes CE = "1", hence enabling the clock oscillator. The debounce counter is then clocked by the system clock until the valid data condition is recognized. Data is then written into the on-chip RAM. CE is maintained at logic "1" by M1 during dialling.

The WRITE ADDRESS COUNTER is reset on recognition of the first valid debounced keyboard input provided that it is decoded during t_d of the pre-impulsing pause PIP (see Figure 8). In the CE INTERNAL CONTROL MODE this condition will always apply. When all keyed digits have been dialled, M1 goes to logic "0" and hence the chip returns to the static standby condition. If digits are subsequently keyed during the same OFF-hook period, after a pause in dialling for example, the digit string will be recognized as a new number. This is not important provided RE-DIAL operation is not required.

The alternative to the CE INTERNAL CONTROL MODE is to override the internal logic gate with an externally derived signal. This mode of operation is referred to as the CE EXTERNAL CONTROL MODE. Figure 7 shows that if CE goes to logic "1" in the absence of a keyboard input, a single pulse of duration t_d is generated on M1. This pulse is intended to initialize a bistable latching relay used as shown in Figure 12. Immediately prior to M1 going to logic "1", the WRITE ADDRESS COUNTER is reset. All digits keyed subsequently are entered into consecutive RAM locations up to a maximum of 20. After the WRITE ADDRESS COUNTER has been reset, the RE-DIAL input code will not be recognized by the circuit. It is necessary that CE be maintained at logic "0" $>$ 1 μs after V_{DD} is applied in order to ensure correct system initializing. If CE is linked to V_{DD} by the method shown in Figure 12, adequate delay is obtained.

3.0 Data Entry – Data is entered to the circuit via a double contact keyboard connected as shown in Figure 10. Keyboard inputs are active low and encoded as shown in Table 2.

Keyboard Code
Table 2

No. of O/P Pulses	Digit	Y_1	Y_2	Y_3	Y_4	X_1	X_2	X_3
1	1	0	1	1	1	0	1	1
2	2	0	1	1	1	1	0	1
3	3	0	1	1	1	1	1	0
4	4	1	0	1	1	0	1	1
5	5	1	0	1	1	1	0	1
6	6	1	0	1	1	1	1	0
7	7	1	1	0	1	0	1	1
8	8	1	1	0	1	1	0	1
9	9	1	1	0	1	1	1	0
10	0	1	1	1	0	1	0	1
RE-DIAL		1	1	1	0	1	1	0

NOTE: "0" indicates pin taken low.

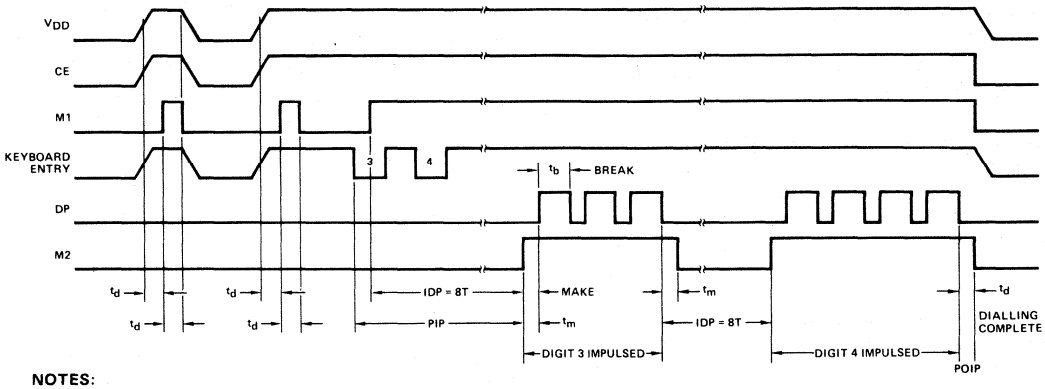
Keyboard inputs are fully decoded eliminating any possibility of invalid codes being recognized. A BCD format is used on-chip for data storage. Valid inputs have contact bounce removed via the debounce counter. Operation is illustrated in Figure 9. Input data is not written into the RAM until the input code has been present for a minimum of 3P and maximum of 4P (P = System Clock Period). The 1P uncertainty arises since data entry is not synchronized to the system clock. This is indicated by the shaded area on the keyboard entry waveform of Figure 9. The trailing edge of a keyboard entry is also debounced. The operation

FUNCTIONAL DESCRIPTION (Cont'd)

of the debounce circuitry results in a maximum data entry rate of SYS CLK ÷ 9. Referring to Figure 9, data must remain stable during the RAM data entry period. Maximum contact bounce rejection is 10 ms at 10 Hz, 6.3 ms at 16 Hz or 5 ms at 20 Hz impulsing rates. Minimum data valid time is 16.7 ms at 10 Hz, 10.4 ms at 16 Hz or 8.4 ms at 20 Hz impulsing rates.

On the DF321, FD is provided to inhibit the debounce circuitry and allow "fast" data entry. When FD = "1", valid keyboard codes may be entered at a maximum rate defined by a data valid time of 2P and an interval between data entry of 1P. This is equivalent to 200 Hz at the 20 Hz impulsing rate. Data need not be synchronized to the system clock since synchronization is provided on-chip.

Upon recognition of the first keyboard input of a number string, the dial out sequence is initiated by a pre-impulsing pause (Figure 7). The WRITE ADDRESS COUNTER is incremented on each digit entry. The contents of this counter indicate the length of the number to be dialled. The RE-DIAL code is recognized only if it is presented to the chip a maximum of 5P after CE = "1". Decoding of RE-DIAL then inhibits the reset of the WRITE ADDRESS COUNTER, initiates the dialling sequence and the previous number string entered is dialled. If the circuit application is to utilize RE-DIAL, external CE control is necessary in some cases to ensure that CE = "1" from the first keyboard entry throughout dialling in order to ensure all digits entered are stored consecutively should a delay occur during dialling.



NOTES:

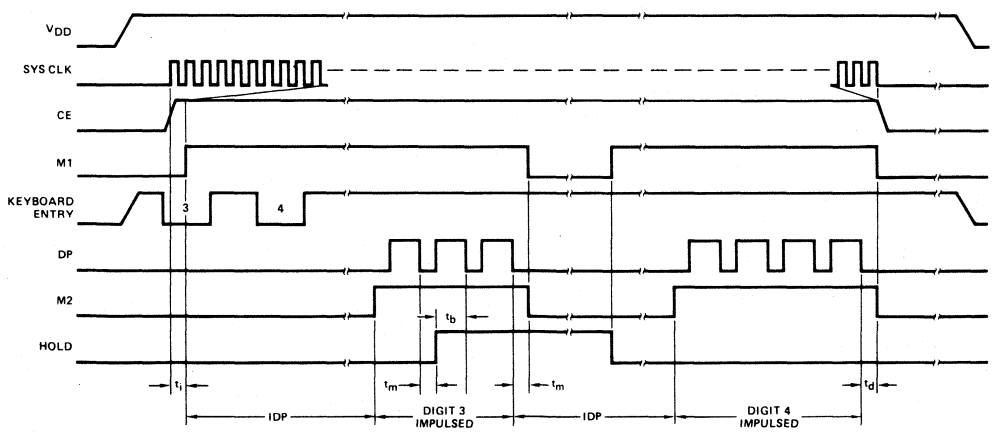
(1) t_d = 10 x P
P = System clock period = T/30
T is selected impulsing period

(2) Pre-Impulsing Pause (PIP) = [(8T or 4T) + t_d]

(3) Post-Impulsing Pause (POIP) is equal to t_d ms

(4) t_b/t_m is the BREAK/MAKE RATIO. T = (t_m + t_b) ms.
t_m = 10 x P for 2:1 M/S ratio. t_m = 12 x P for 3:2 M/S ratio.

Loop Disconnect Dialler Timing Diagram CE—External Control
Figure 7



NOTE:

(1) $t_i = t_{ON} + t_d$ where t_{ON} = Clock Start Up Time

Loop Disconnect Dialler Timing Diagram CE—Internal Control
Figure 8

FUNCTIONAL DESCRIPTION (Cont'd)

4.0 Dialling Sequence – The dialling or impulsing sequence is initiated on recognition of the first keyboard entry after CE = "1". The dialling sequence is identical for both internal and external control of CE. (See Figure 7 and 8).

The basic impulsing pulse train is derived from the TIMING COUNTER AND DECODE. The IDP is timed by forcing a code on the OUTPUT COUNTER and inhibiting DP for the duration of IDP. The READ ADDRESS COUNTER then addresses the RAM and the first digit is used to program the decode of the OUTPUT COUNTER. A number of dial pulses is output via DP corresponding to the BCD data read from the RAM. At the completion of the digit, the READ ADDRESS COUNTER is incremented. The sequence continues until coincidence is recognized between the READ ADDRESS COUNTER contents and the WRITE ADDRESS COUNTER contents. The post-impulsing pause POIP, is then generated. The circuit then enters the dynamic standby condition if CE is maintained at logic "1" by external control, or the static standby condition if CE INTERNAL CONTROL MODE is used.

Impulsing rates, impulsing mark-to-space ratio and inter-digital pause are programmable as shown in Table 1.

The dialling sequence can be interrupted by applying logic "1" to HOLD. If HOLD = "1" is applied during dialling of a digit, the circuit does not enter the HOLD mode until the digit is complete. In the HOLD mode M1 = "0", allowing the telephone line to be monitored. When HOLD is released dialling continues preceded by an IDP. (See Figure 8). HOLD is used to extend the IDP allowing intermediate dial tone recognition if RE-DIAL is used in a PABX for example. Operation can be manual or via external control logic as shown in Figure 13.

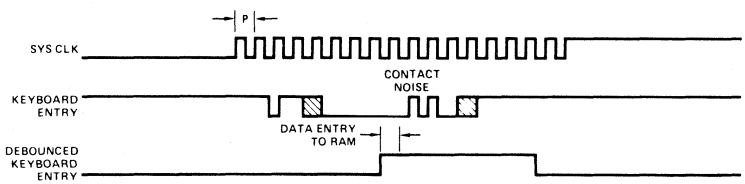
NOTES:

(1) The keyboard input decoding is mask programmable to suit different input codes.

(2) The timing circuitry is mask programmable to give different M/S ratios.

(3) The clock predivision circuitry is mask programmable allowing use of different crystal or external clock frequencies.

(4) The logic sense of DP, M1 and M2 outputs is mask programmable.



Keyboard Input Debounce Timing Diagram
Figure 9

APPLICATIONS

The circuit of Figure 10 shows a method of connecting the DF320 in parallel with the telephone network.

When the handset is lifted and power applied to the circuit Q_2 is fed base current through R_2 which in turn drives Q_1. C_2 is charged via R_3 in series with D_1 to $(V_{Z1} - 0.7)V$. When the minimum operating V_{DD} voltage is reached, power ON reset occurs via the CE network of C_1 and R_8. Q_2 is maintained in the ON condition by G_1 while Q_3, and hence Q_4, are held OFF by G_2. The DF320 network appears in parallel with the telephone as an impedance $>$ 10K Ω in the standby condition with the telephone network connected in circuit through Q_1.

On recognition of the first keyed digit, the DF320 clock is started. M1 then goes to logic "1" causing Q_2, Q_1 to turn OFF, and Q_3, Q_4 to turn ON. Hence the majority of the line loop current now flows through Q_4, and Z_1. When impulsing occurs Q_3 and Q_4 are turned OFF by DP acting on G_2. Line loop current is then reduced to approximately 50 μA taken through R_2, R_4 and G_2 in series.

When dialling is complete M1 goes to logic "0" causing the telephone network to be reconnected. The DF320 then returns to the static standby condition. If the line loop is interrupted by the cradle switch during dialling, impulsing will continue until C_2 discharges to a voltage such that R_8 pulls CE to logic "0" causing the DF320 to reset.

The diode bridge protects the network from line polarity reversal.

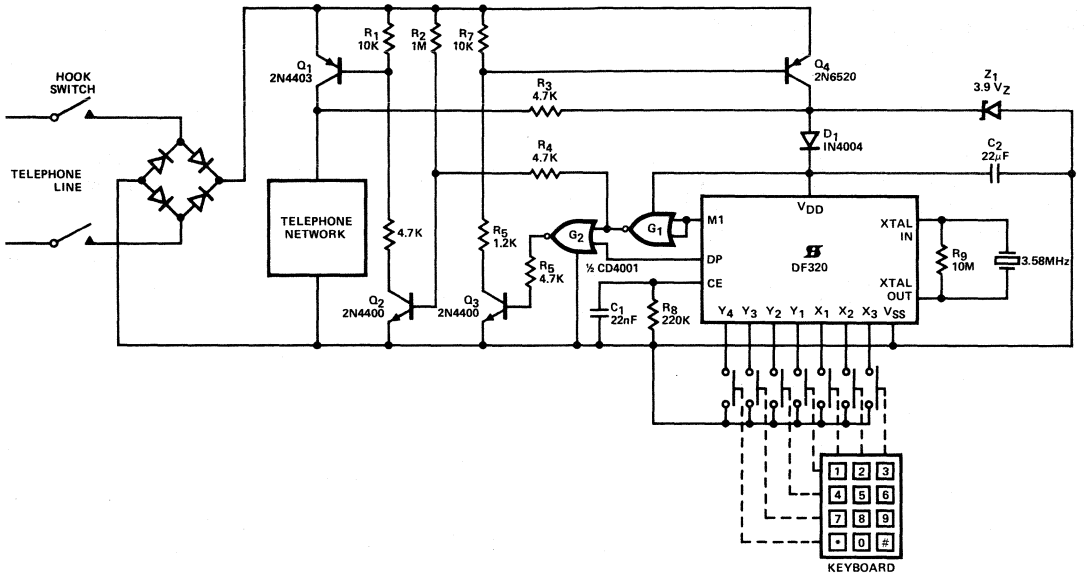
The circuit of Figure 11 shows a simple method of series connection of DF320 into the telephone set suitable for PABX or short line applications.

APPLICATIONS (Cont'd)

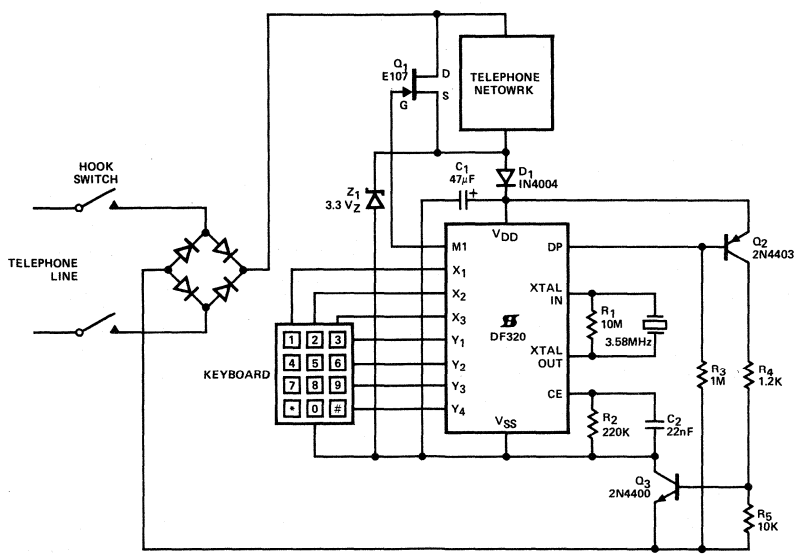
When the telephone handset is lifted, C_1 is charged via D_1 to (V_{Z1} – 0.7) volts and DF320 power ON reset occurs. When the first keyed digit is recognized, M1 goes to logic "1" muting the telephone network by switching on the low ON resistance JFET Q_1, and maximizing the line loop current for impulsing. Impulsing occurs through DP switching Q_2, and hence Q_3, OFF. Rapid discharge of C_1 through Z_1 is prevented during line break by the blocking diode D_1.

When dialling is complete the circuit returns to the static standby condition and Q_1 is switched OFF. Circuit reset during a line interruption by the cradle switch is as for the parallel connection mode.

If a requirement exists that no semiconductor components should appear in the telephone loop during normal speech, the circuit of Figure 12 is required.



DF320 Parallel Telephone Connection
Figure 10



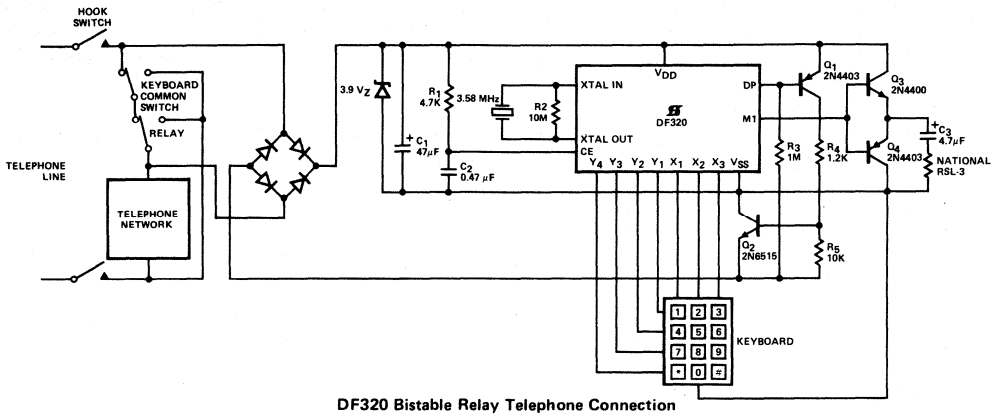
DF320 Series Telephone Connection
Figure 11

APPLICATIONS (Cont'd)

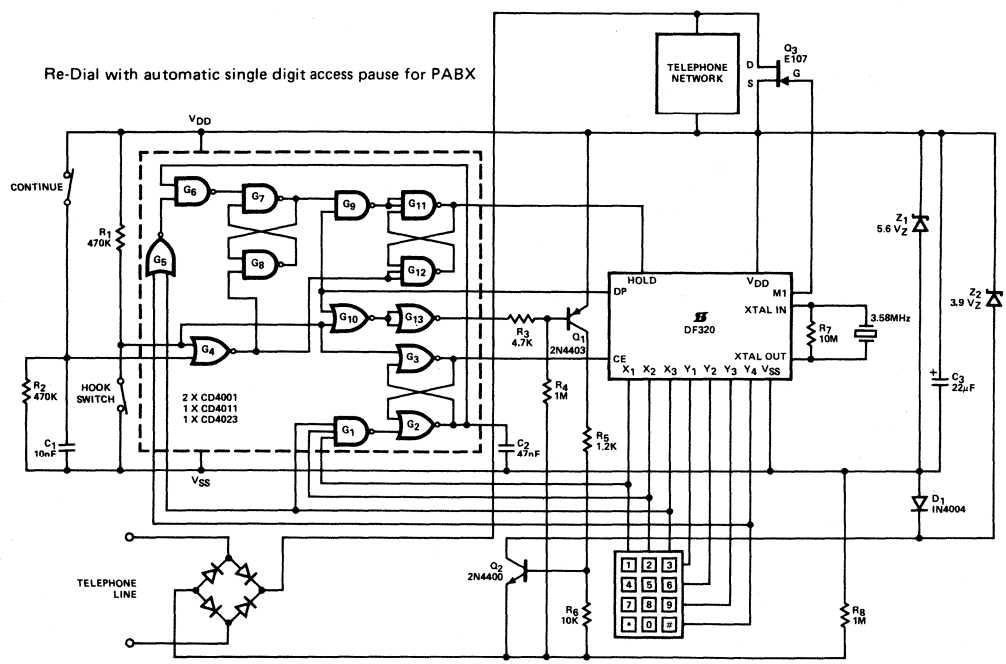
While the circuits of Figures 10 and 11 did not require a common keyboard contact, it is necessary to have a common changeover switch in this case operating in conjunction with a bistable relay. In this application external control of CE is provided by the R_1, C_2 network. If, when the handset is lifted, the relay contact is such that the DF320 network is connected in circuit, it is necessary to initialize this relay to reconnect the telephone network. This is achieved by the single pulse which occurs on M1 if CE goes to logic "1" in the absence of a keyboard input (Figure 7).

When the first digit is keyed, the DF320 network is connected into the telephone loop and the telephone network short circuited by the keyboard common switch. M1 then goes to logic "1" switching the bistable relay hence maintaining the DF320 network in circuit. Impulsing occurs through DP switching Q_1 OFF which in turn switches Q_2. When dialling is complete the bistable relay is pulsed, switching the telephone network back in circuit and short circuiting the DF320 network.

The circuit of Figure 13 shows additional gating circuitry to provide an automatic access pause after the first digit is dialled, by controlling HOLD. This is useful in PABX applications, eliminating the need for a manual hold facility if RE-DIAL is used.



DF320 Bistable Relay Telephone Connection
Figure 12



DF320 Series Telephone Connection
Figure 13

APPLICATIONS (Cont'd)

The basic interface circuit is similar to that shown in Figure 11. Muting is achieved by Q_3 and line switching by Q_2 driven by Q_1.

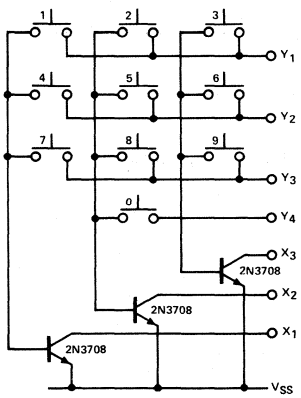
In the ON-hook condition, Q_1 is held OFF by G_{13} and standby current is supplied to the DF320 network by R_8; providing voltage limiting. CE is clamped to logic "0" by G_3. The DF320 is in the static standby mode and the previously dialled number is stored.

When the handset is lifted, G_{13} goes to logic "0" switching Q_1, and hence Q_2, ON. The DF320 network V_{DD} is now given by (V_{Z2} − 0.7) volts. The DF320 remains in the static standby mode until the first key operation. G_1 decodes the common key function toggling the latch formed by G_2 and G_3 causing CE = "1". CE remains at logic "1" throughout the remainder of the OFF-hook condition ensuring that all digits keyed are stored by the DF320 as one number string. (See FUNCTIONAL DESCRIPTION, 3.0 DATA ENTRY).

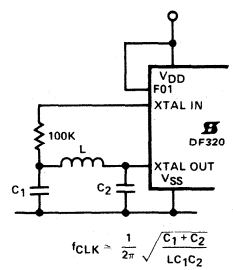
If the first key operated is RE-DIAL, this condition is decoded by G_5, and via G_6 sets the latch formed by G_7 and G_8. G_9 is enabled and the first dial pulse causes the latch formed by G_{11} and G_{12} to be set taking HOLD to logic "1". When the first digit is complete M1 goes to logic "0" enabling the telephone network. When dial tone is recognized the CONTINUE switch is operated causing HOLD = "0" by resetting the latches formed by G_{11}, G_{12} and G_7, G_8. The remainder of the number is then re-dialled. Subsequent operation of RE-DIAL is blocked by G_6.

Figure 14 shows a simple method of interfacing a single contact matrix-type keyboard to the DF320 (DF321, DF322). Operation of a key causes the on-chip pull-up transistor of the Y input to provide base drive current to the corresponding X input external bipolar transistor, which sinks the X input pull-up current through its collector. Hence, a valid code is presented.

As an alternative to the crystal oscillator it is possible to operate the DF320 (DF321, DF322) from an LC combination connected as shown in Figure 15. F01 is connected to V_{DD} selecting the 932 Hz impulsing condition. An oscillator frequency of 38.4kHz will give a 10 Hz impulsing rate.



Single Contact Keyboard Interface
Figure 14



LC Oscillator
Figure 15

CMOS μ-255 law CODEC set

designed for . . .

- **Channel Banks**
- **Central Offices and PABXs**
- **Microprocessor Interface**
- **Remote Data Acquisition Systems**
- **Audio Delay Lines**

Siliconix

BENEFITS

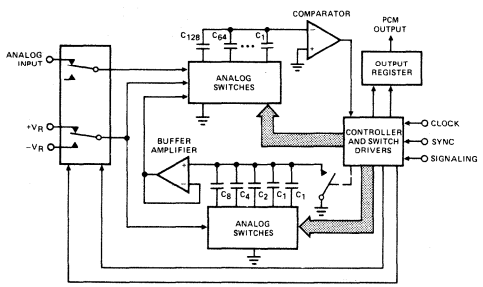
- **Minimizes System Power Requirements**
  - Standby Power 11 mW Typ
  - Typical Power 80 mW
- **Reduces External Component Requirements**
- **Reduces System Costs**
- **Easily Interfaced**
- **Eliminates Channel Crosstalk Problems**
- **Eliminates External Signalling Logic**
- **No External Zero Code Suppression Required**
- **Reduced System Noise Problems**
- **No External Sample and Hold or MUX Required**
- **No Additional Logic Required for Extended Bandwidth Applications**
  - 3.5 to 9 KHz Bandwidth Possible With Clock Frequency From 1.25 to 3.0 MHz

DESCRIPTION

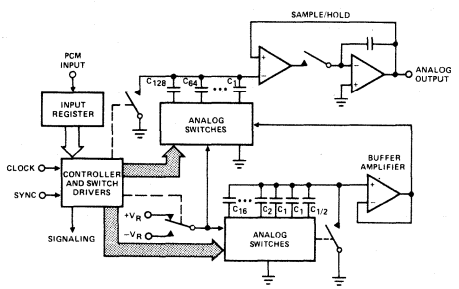
The DF331A (coder) is an A/D converter which has a transfer characteristic conforming to the telecommunication industry μ-255 law. Its counterpart, the DF332A or DF334A (decoder) is a D/A converter which also conforms to the μ-255 law.

Together the DF331A and DF332A or DF331A and DF334A form a CODEC (coder-decoder set) which is designed to meet the needs of the telecommunications industry for per channel voice frequency CODECs used in PCM Channel Bank and PBX systems. Digital output and input of the coder and decoder is in serial format. Actual transmission and reception of 8-bit data words containing the analog information is typically done at a 1.544 megabit/sec rate with analog signal sampling occurring at an 8 KHz rate. A sync pulse input pin is provided for synchronizing transmission and reception of multi-channel information being multiplexed over a single transmission line. The DF332A and DF334A differ in the output device for the A/B signal output pins, refer to the Functional Description. The devices have TTL logic input levels of 0.6 V and 3.4 V that are compatible with TTL logic using a pullup resistor to +5 V; they directly interface to CMOS logic.

FUNCTIONAL BLOCK DIAGRAMS



DF331A

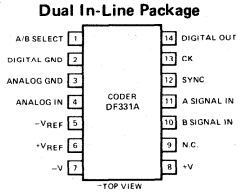


DF332A, DF334A

Figure 1

PIN CONFIGURATIONS

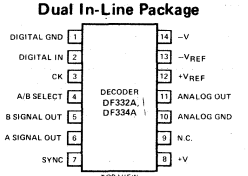
Dual In-Line Package



PLASTIC DIP
ORDER NUMBER: DF331ACJ
SEE PACKAGE 7

CERAMIC DIP
ORDER NUMBER: DF331ACP
SEE PACKAGE 11

Dual In-Line Package



PLASTIC DIP
ORDER NUMBER: DF332ACJ, DF334ACJ
SEE PACKAGE 7

CERAMIC DIP
ORDER NUMBER: DF332ACP, DF334ACP
SEE PACKAGE 11

ABSOLUTE MAXIMUM RATINGS

V_{in} (Digital Inputs) . . . . $-0.3\ V, \leq V_{in} \leq +V + 0.3\ V$
V_{in} (Analog Inputs) . . . $-V - 0.3\ V, \leq V_{in} \leq +V + 0.3\ V$
$+V$ . . . . . $0 \leq +V \leq 11\ V$
$-V$ . . . . . $-11\ V \leq -V \leq 0$
$+V_{ref}$ . . . . . $-V \leq +V_{ref} \leq +V$
$-V_{ref}$ . . . . . $-V \leq -V_{ref} \leq +V$

V_o (Digital Output) DF331A, DF334A . . $-0.3V \leq V_o \leq 15V$
$V_{A/B}$ Signal Out DF332A . . . $+V + 0.3\ V \geq V_o \geq -7.5\ V$
Operating Temperature . . . . . 0 to 70°C
Storage Temperature . . . . . −55 to +125°C
Power Dissipation . . . . . 450 mW
Derate 6.5 mW/°C above 25°C

Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters to assure conformance with specifications.

		Characteristic		$T_A = 25°C$ Min	Typ Note 1	Max	Unit	Test Conditions, See Note 2 Clock = 1.544 MHz, Sample Rate = 8 KHz, $+V = 7.5\ V$, $-V_{ref} = -3.0\ V$, $-V = -7.5\ V$, $+V_{ref} = 3.0\ V$, $R_L = 820\ \Omega$, $C_L = 12.5\ pF$
DC Characteristics DF331A (Coder)								
1	INPUTS	I_{in} (Analog)	Analog Input Current		0.5		mA	See Note 3
2		I_{inL} (Clock)	Clock Input Low Current		−0.1	−100	nA	$V_{IN} = 0$
3		I_{inL} (Sync)	Sync Input Low Current		−0.1	−100		
4		I_{inH} (Clock)	Clock Input High Current		0.1	100		$V_{IN} = 7.5\ V$
5		I_{inH} (Sync)	Sync Input High Current		0.2	100		
6		R_{in} (Analog)	Analog Input Series Resistance		1		KΩ	Present During Sampling Time Only
7		C_{in} (Analog)	Analog Input Series Capacitance		200		pF	
8		V_{offset}	Analog Input Offset Voltage		5	10	mV	
9	OUT	C_o (Digital)	Digital Output Capacitance		3		pF	$V_o = 7.5\ V$
10		V_{OL}	Digital Output Low Voltage		0.3	0.5	V	$I_{OL} = 3\ mA$
11		V_{OH} (max)	Digital Output High Voltage			12		$I_{OH} = 10\ \mu A$
12	SUPPLY	I^+	Positive Supply Current		2.5	6	mA	Clock = 1.544 MHz Sample Rate = 8 KHz
13		I^-	Negative Supply Current		−2	−6		
14		I^+_{stdby}	Standby Positive Supply Current		0.6			Analog Ground (Pin 3) Open
15		I^-_{stdby}	Standby Negative Supply Current		−0.05			
16			Supply Tolerance		±10		%	
17		I_{ref}^+	Positive Reference Current		3.5		μA ·	Average Current See Note 3
18		I_{ref}^-	Negative Reference Current		−3.5			
AC Characteristics DF331A (Coder)								
19	DYNAMIC	$\|t_{ds}\|$	Sync to Clock Delay Time			100	ns	See Figure 2
20		$t_{d(on)}$	Digital Output to Sync Delay Time		75	130		
21		$t_{d(off)}$	Digital Output to Sync Delay Time		165	220		
22		t_{dbr}	Digital Output to Clock Delay Time		65	130		
23		t_{dbf}	Digital Output to Clock Delay Time		70	130		
24		t_{fo}	Digital Output Fall Time		65	130		$C_L = 100\ pF$
25		t_{ro}	Digital Output Rise Time		175	250		
26		t_{ss} (min)	A/B Signaling Input Setup Time			200		See Figure 4
27		t_{scs} (min)	A/B Select Setup Time			1000		
28		DC_c	Clock Duty Cycle	30		70	%	
29		t_{conv}	Complete A/D Conversion (Sampling, Data Storage, Resetting)			168	clocks	

ELECTRICAL CHARACTERISTICS (Cont'd)

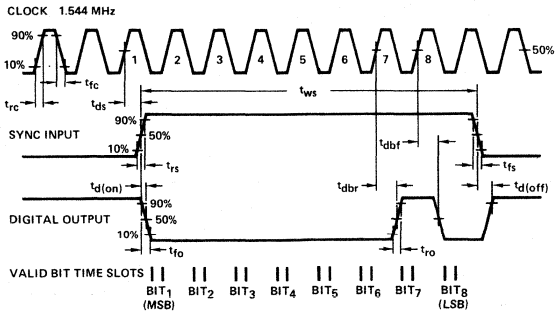
All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters to assure conformance with specifications.

		Characteristic			T_A = 25°C Min	Typ Note 1	Max	Unit	Test Conditions, See Note 2 +V = 7.5 V, −V = −7.5 V, V_{ref} = 3.0 V, $-V_{ref}$ = −3.0 V, Clock = 1.544 MHz, Sync = 8 KHz Period, 8 Clock Pulses Wide
DC Characteristics DF332A, DF334A (Decoder)									
1	IN	I_{inL} (Logic)	Digital Inputs Low Current			−0.1	−100	nA	V_{in} = 0
2	IN	I_{inH} (Logic)	Digital Inputs High Current			0.1	100	nA	V_{in} = 7.5 V
3	OUT	I_{OL} (Signaling)	A/B Output Low Current	DF332A Only		0.1	100	nA	V_{OL} = 0
4	OUT	I_{OH} (Signaling)	A/B Output High Current	DF332A Only	0.2	0.5		mA	V_{OH} = 6.5 V
5	OUT	V_{OH} (max) (Signaling)	A/B Output High Voltage	DF334A Only			12	V	I_{OH} = 10 μA
6	OUT	V_{OL} (Signaling)	A/B Output Low Voltage	DF334A Only		0.3	0.5	V	I_{OL} = 1.5 mA
7	OUT	C_L (Analog)	Analog Output Load Capacitance				100	pF	
8	OUT	R_O (Analog)	Analog Output Series Resistance			50	150	Ω	See Input/Output Schematics, See Note 4
9	OUT	V_{offset}	Analog Output Offset Voltage			50	100	mV	
10	SUPPLY	I^+	Positive Supply Current			3.5	8	mA	
11	SUPPLY	I^-	Negative Supply Current			−2.5	−7	mA	
12	SUPPLY	I^+_{stdby}	Standby Positive Supply Current			0.8		mA	Analog Ground (Pin 10) Open
13	SUPPLY	I^-_{stdby}	Standby Negative Supply Current			−0.07		mA	Analog Ground (Pin 10) Open
14	SUPPLY		Supply Tolerance			±10		%	
15	SUPPLY	$I_{ref}{}^+$	Positive Reference Current			3.5		μA	Average Current See Note 3
16	SUPPLY	$I_{ref}{}^-$	Negative Reference Current			−3.5		μA	Average Current See Note 3
AC Characteristics DF332A, DF334A (Decoder)									
17	DYNAMIC	t'_{ds}	Sync to Clock Delay Time		25		450	ns	See Figure 3
18	DYNAMIC	t'_{dc}	Clock to Sync Delay Time		10			ns	See Figure 3
19	DYNAMIC	t'_{sd}	Data to Clock Setup Time		100			ns	See Figure 3
20	DYNAMIC	t'_{scs} (min)	A/B Select Setup Time				1000	ns	See Figure 5
20	DYNAMIC	t'_d	A/B Output Delay Time			5	10	μs	See Figure 5
21	DYNAMIC	t'_{do}	Analog Output to Sync Delay Time				15	μs	See Figure 3
22	DYNAMIC	$Slew^+$	−3 V to +3 V Analog Output Slew Rate			5		V/μs	C_L = 100 pF
23	DYNAMIC	$Slew^-$	+3 V to −3 V Analog Output Slew Rate			5		V/μs	C_L = 100 pF
24	DYNAMIC	Droop	Analog Output Droop Rate			0.01		%/μs	
25	DYNAMIC	t'_{conv}	Complete D/A Conversion (from Data Input, to Analog Output and Internal Resetting)				39	clocks	
System Characteristics, Per Individual Part: DF331A, DF332A, DF334A									
26	SYSTEM	S/D	Signal to Total Distortion: Total of Quantizing Noise, Thermal Noise and Harmonic Distortion with Sinusoidal Input and C Message Weighting Filter. See Note 5		35	39		dB	P_{in} = 0 to −30 dBmO; f_{in} = 1020 Hz +3 dBmO = 3 V Peak into Coder
27	SYSTEM	S/D	Signal to Total Distortion: Total of Quantizing Noise, Thermal Noise and Harmonic Distortion with Sinusoidal Input and C Message Weighting Filter. See Note 5		30	34		dB	P_{in} = −40 dBmO; f_{in} = 1020 Hz +3 dBmO = 3 V Peak into Coder
28	SYSTEM	S/D	Signal to Total Distortion: Total of Quantizing Noise, Thermal Noise and Harmonic Distortion with Sinusoidal Input and C Message Weighting Filter. See Note 5		25	30		dB	P_{in} = −45 dBmO; f_{in} = 1020 Hz +3 dBmO = 3 V Peak into Coder
29	SYSTEM	G_T	Gain Tracking: Deviation of Gain from 0 dBmO Input Sinusoidal Signal		−0.25	±0.15	+0.25	dB	P_{in} = +3 to −40 dBmO; f_{in} = 1020 Hz +3 dBmO = 3 V Peak into Coder
30	SYSTEM	G_T	Gain Tracking: Deviation of Gain from 0 dBmO Input Sinusoidal Signal		−0.5	±0.15	+0.5	dB	P_{in} = −40 to −50 dBmO; f_{in} = 1020 Hz +3 dBmO = 3 V Peak into Coder
31	SYSTEM	G_T	Gain Tracking: Deviation of Gain from 0 dBmO Input Sinusoidal Signal		−1.5	±0.25	+1.5	dB	P_{in} = −50 to −55 dBmO; f_{in} = 1020 Hz +3 dBmO = 3 V Peak into Coder
	SYSTEM	G_T	Deviation of Gain from −10 dBmO, White Noise Source Signal Input		−0.25	±0.1	+0.25	dB	P_{in} = −10 to −55 dBmO; f_{in} = 1020 Hz +3 dBmO = 3 V Peak into Coder
	SYSTEM	G_T	Deviation of Gain from −10 dBmO, White Noise Source Signal Input		−0.5	±0.2	+0.5	dB	P_{in} = −55 to −60 dBmO; f_{in} = 1020 Hz +3 dBmO = 3 V Peak into Coder
32	SYSTEM	N_{IC}	Idle Channel Noise: Coder (DF331A) to Decoder (DF332A or DF334A) of Known Quiet Code Output			12	15	dBrncO	V_{in} = 0
33	SYSTEM	N_{QC}	Quiet Code Output: Output of Decoder (DF332A or DF334A) for +0 V Equivalent Digital Input Coder			10	12	dBrncO	Digital In = All "1" (Corresponds to +0 V Input)

NOTES:
1. Typical values are for Design Aid only and not subject to production testing.
2. $V_{in} \geq 3.4$ V for logic "1", $V_{in} \leq 0.6$ V for logic "0" for logic input levels.
3. Peak currents of up to 2 mA occur during reconstruction of Analog Output and during encoding of Analog Input.
4. Use of a load resistance ≥ 10K Ω is recommended to avoid output attenuation.
5. Specifications are for pair (coder and decoder)

DF331A ICBL-II
DF332A ICBM-II-A
DF334A ICBM-II-B

SWITCHING AND LOGIC WAVEFORMS



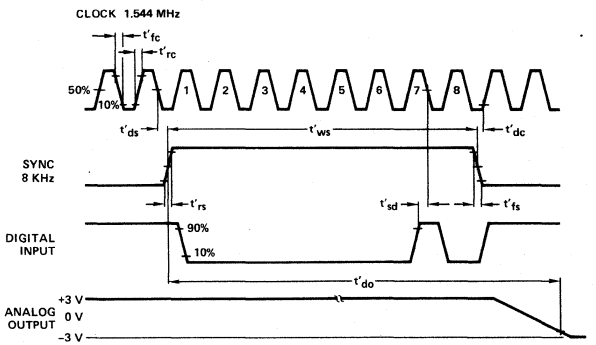
DF331A Coder Waveforms
Figure 2A

	Parameter	Test Condition	Min	Max	Unit
t_{rc}	Clock Rise Time	50		100	ns
t_{fc}	Clock Fall Time	50		80	
t_{rs}	Sync Rise Time	50		100	
t_{fs}	Sync Fall Time	50		100	
t_{ws}	Sync Pulse Width	5.18	$8/F_{CLOCK}$		µs
t_{ps}	Sync Pulse Period	125			

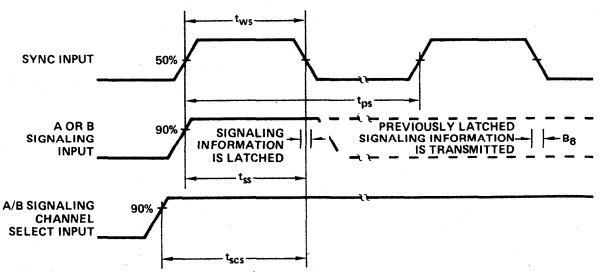
DF331A Coder Waveforms
Figure 2B

	Parameter	Test Condition	Min	Max	Unit
t'_{rc}	Clock Rise Time	50		100	ns
t'_{fc}	Clock Fall Time	50		80	
t'_{rs}	Sync Rise Time	50		100	
t'_{fs}	Sync Fall Time	50		100	
t'_{ws}	Sync Pulse Width	5.18	$8/F_{CLOCK}$		µs
t'_{ps}	Sync Pulse Period	125			

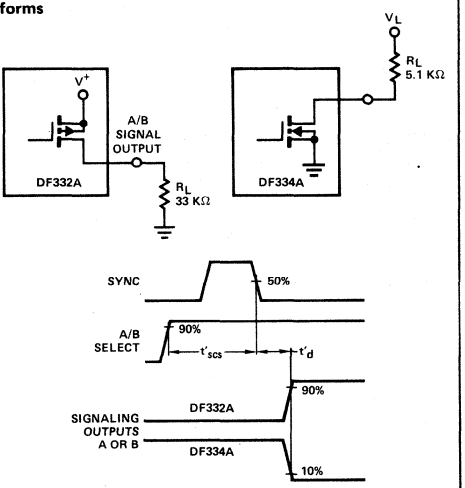
DF332A, DF334A Decoder Waveforms
Figure 3B



DF332A, DF334A Decoder Waveforms
Figure 3A



DF331A Signaling Waveforms
Figure 4



DF332A, DF334A Signaling Waveforms
Figure 5

FUNCTIONAL DESCRIPTION

Analog Input (Coder DF331A): The analog input accepts signals which have peak amplitudes less than the value of the voltage references, and which are bandlimited to less than 1/2 of the CODEC sample rate.

Digital Output (Coder DF331A): The digital output of the encoder is an 8-bit serial bit stream which is a sign-plus-magnitude binary representation of the analog input. This output is an open drain N-channel output, which allows for easy wire-OR multiplexing.

Sync Input (Coder and Decoder): The sync input accepts a sync pulse which should be 8 clock periods wide. The period of the sync pulse sets the sample rate. The sync pulse causes the encoder to serially shift its digital output data out at a rate equal to that of the clock, and it causes the decoder to accept the serial digital data.

Clock Input (Coder and Decoder): The clock input accepts a clocking signal which sets the data transmission rate for the CODEC, and also provides the clocking of the internal CODEC logic. Typical clock rate is 1.544 MHz.

Digital Input (Decoder DF332A, DF334A): The digital input accepts the 8-bit serial data output of the encoder upon reception of the sync pulse.

Analog Output (Decoder DF332A, DF334A): The analog output of the decoder is in the form of voltage steps having a width equal to the inverse of the sample rate, with amplitude equal to the value of the sample of the signal taken at the encoder analog input.

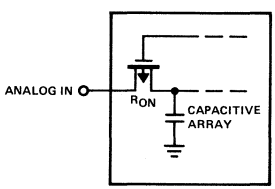
Reference Voltage Inputs (Coder and Decoder): Positive and negative DC reference voltages are required for both encoding and decoding. The maximum analog signal swing is set by the reference voltages.

Signaling Inputs and A/B Select (Coder DF331A): Two signaling inputs A and B are provided on the encoder allowing insertion of digital signaling data into the transmitted bit stream, which allows telecommunications users to transmit digital signaling information along with the data stream. When signaling is enabled, the voice signal is encoded with only 7 bits, the 8th bit being used for signaling. The signaling function is enabled by the application of a transition to the A/B select input. A positive transition at the A/B select input will insert the data at the A input into the 8th bit (the LSB) position in the transmitted word, whereas a negative transition will insert the data at the B input into the 8th bit position in the transmitted word. Refer to the timing diagram in Figure 4. To disable signaling function, simply tie the A/B select input to logic high or low, so that no transitions appear.

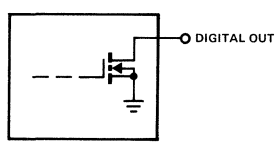
Signaling Outputs and A/B Select (Decoder DF332A, DF334A): Two outputs are provided on the decoder to output the signaling data. Application of a positive transition to the A/B select input places the 8th bit (the LSB) of the transmitted word at the A signaling output. Application of a negative transition to the A/B select input places the LSB at the B signaling output. These outputs are open drain P-channel outputs on the DF332A and are open drain N-channel outputs on the DF334A. Refer to output schematic for configuration, and to Figure 5 for timing waveforms.

INPUT-OUTPUT CIRCUIT SCHEMATICS

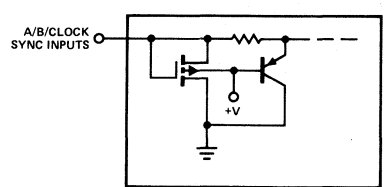
Analog Input (DF331A)



Digital Output (DF331A)

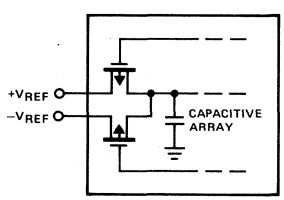


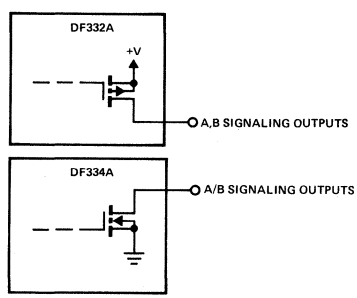
Digital Inputs



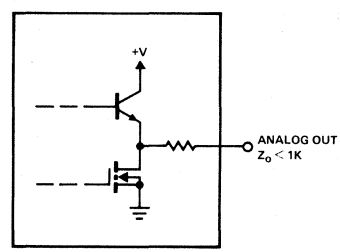
A/B Signaling Outputs (DF332A, DF334A)

Reference Inputs



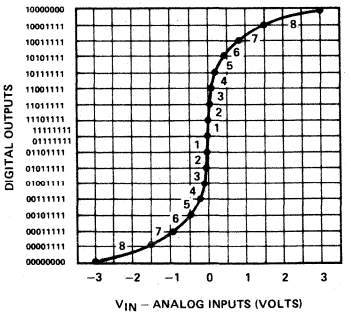


Analog Output (DF332A, DF334A)

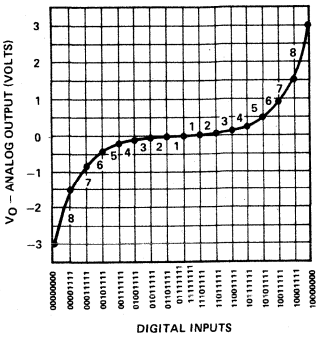


TYPICAL CHARACTERISTICS

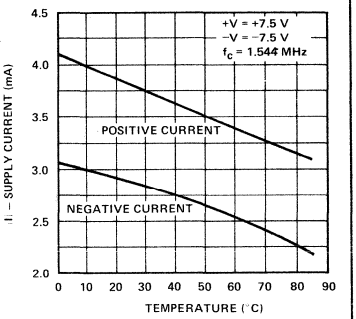
DF331A μ-Law Coder Transfer Characteristic



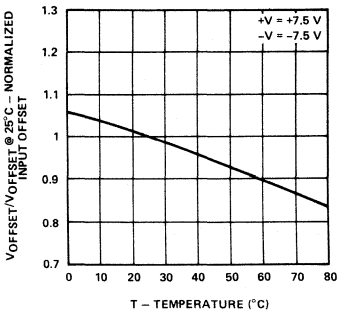
DF332A μ-Law Decoder Transfer Characteristic



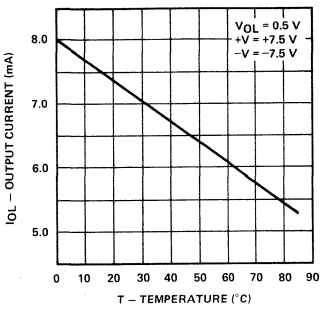
Positive and Negative Supply Current vs Temperature DF331A



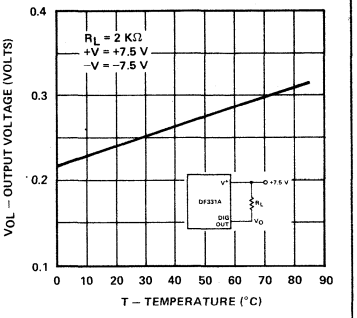
Normalized Input Offset vs Temperature DF331A



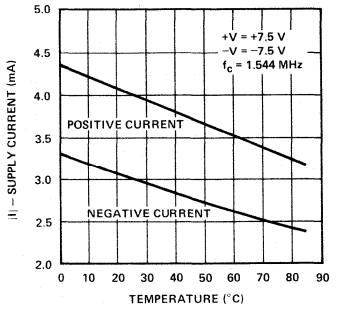
Digital Output Low Current vs Temperature DF331A



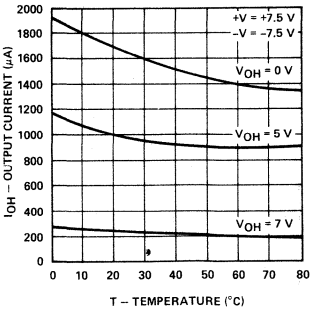
Digital Output Low Voltage vs Temperature DF331A



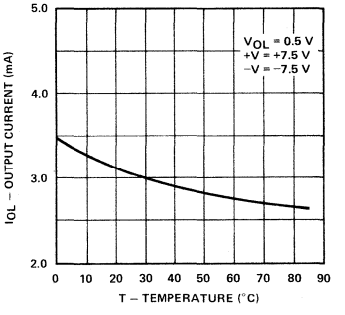
Positive and Negative Supply Current vs Temperature DF332A, DF334A



A/B Signaling Output Current vs V_{OH} and Temperature DF332A Only

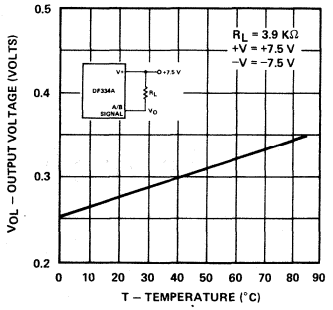


A/B Signaling Digital Output Low Current vs Temperature DF334A

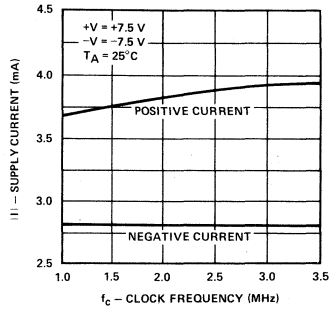


TYPICAL CHARACTERISTICS (Cont'd)

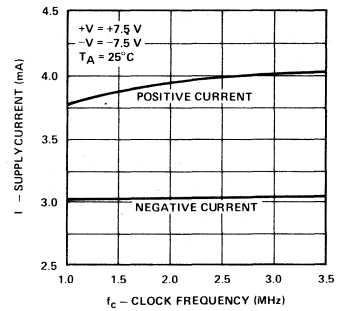
A/B Signaling
Digital Output Low Voltage
vs Temperature
DF334A



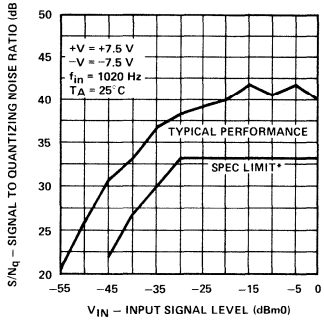
Positive and Negative
Supply Current
vs Clock Frequency
DF331A



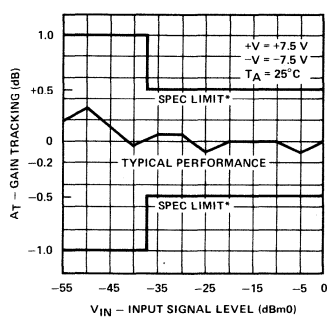
Positive and Negative
Supply Current
vs Clock Frequency
DF332A, DF334A



Signal to Quantizing Noise Ratio
vs Input Level
DF331A/DF332A or DF331A/DF334A Pair



Gain Tracking
vs Input Level
DF331A/DF332A or DF331A/DF334A Pair



*SPECIFICATION LIMITS FROM A.T.T. CHANNEL BANK D-3 SPEC

APPLICATIONS INFORMATION

Positive and negative voltage references should be bypassed to analog ground with a 10 μF capacitor to supply the peak currents required (up to 2 mA) during sampling. Inadequate bypassing may cause sampling inaccuracy and crosstalk between adjacent channels. The absolute value of the voltage references should match and track each other to prevent asymmetry in the analog waveforms. The recommended reference value is ±3.0 V. Increasing this level may increase harmonic distortion in the CODEC, while decreasing the references will lower the system dynamic range.

The sync pulses to the decoder and encoder should be staggered as in Figure 6. The sync to the decoder precedes the sync to the encoder by one half of a clock period to allow for the delay times which can occur if the sync pulse is derived from the clock. If all syncs and clocks are coincident without delay, then the staggering is unnecessary.

All digital inputs will work when driven from TTL logic providing that the outputs of the TTL gates are pulled up to the 5.0 V TTL supply.

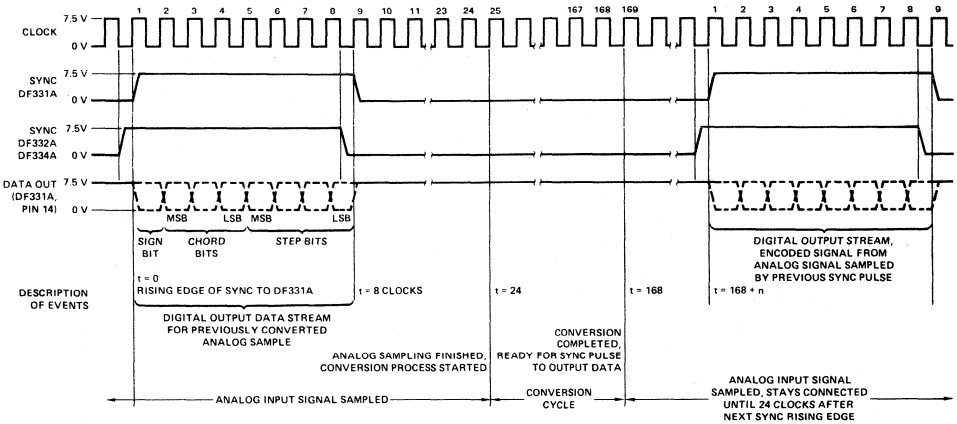
The sample rate of the CODEC is determined by the clock rate and the period between sync pulses. The minimum period between sync pulses is 168 clock periods, which is the time that the encoder requires to complete an analog-to-digital conversion (see Figure 6). The maximum clock rate for a functional system is 3.0 MHz. The actual sample rate of the CODEC is equal to the inverse of the period between sync pulses.

Zero code suppression is included in the A/D conversion to prevent the transmission of an all zeroes digital output code, which could cause a repeater to go down in a telecommunications system. Should an all zeroes code result from the A/D conversion (indicating a negative overvoltage condition), then bit 7 in the data stream is forced to a logic "1".

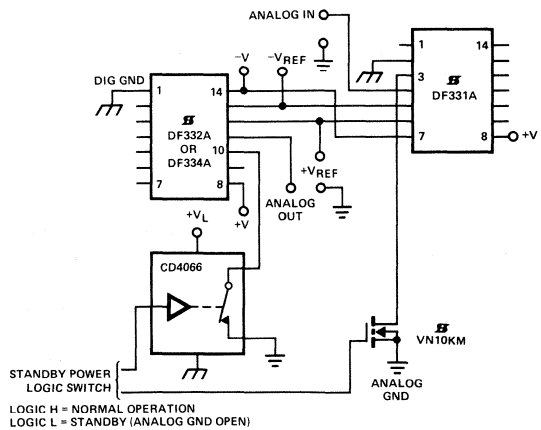
Open drain signaling outputs on the decoder allow easy interface to logic. The open drain P-channel of the DF332A allows a pull-down to ground or a negative voltage ($V_O \geq$ −7.5 V absolute max) giving logic compatibility with CMOS or other MOS logic. The open drain N-channel of the DF334A allows a pull-up to a positive supply (e.g., +5 V for TTL or up to +12 V for CMOS). This output has logic low level near ground making it compatible with TTL or CMOS logic.

APPLICATIONS INFORMATION

The CODECs can be put into a lower power standby condition. For standby, analog ground lines are open circuited. Relays or FET switches can be used. Figure 7 shows one implementation for standby switching. For the encoder (DF331A) the switch must be low $R_{DS(ON)}$ (<25 Ω) and have very low total offset voltage (<5 mV at 200 μA current). The VMOS switch shown (VN10KM) achieves these requirements. The decoder is not as critical, offset voltage should be minimized (<50 mV); use of a CD4066 CMOS switch is satisfactory.



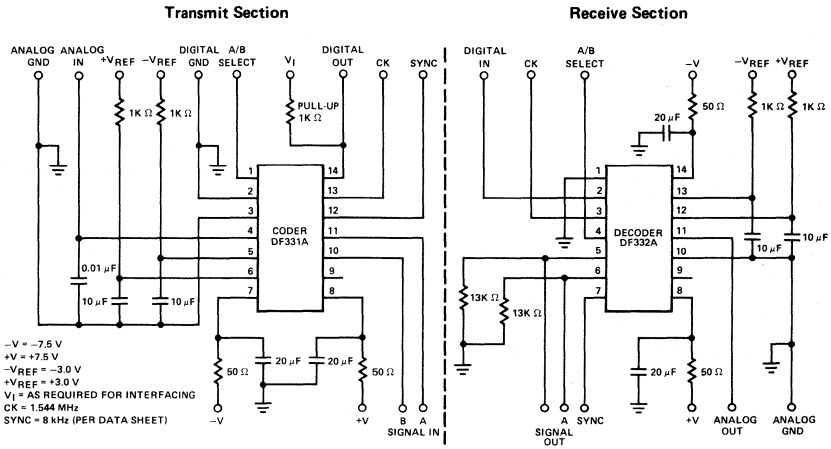
CODEC Timing Relationships
Figure 6



Coder/Decoder Circuit with Switches for Standby Power Condition
Figure 7

APPLICATIONS

Typical Coder/Decoder Circuit Configurations



CMOS A-law CODEC set

designed for . . .

- **Channel Banks**
- **Central Offices and PABXs**
- **Microprocessor Interface**
- **Remote Data Acquisition Systems**
- **Audio Delay Lines**

Siliconix

BENEFITS

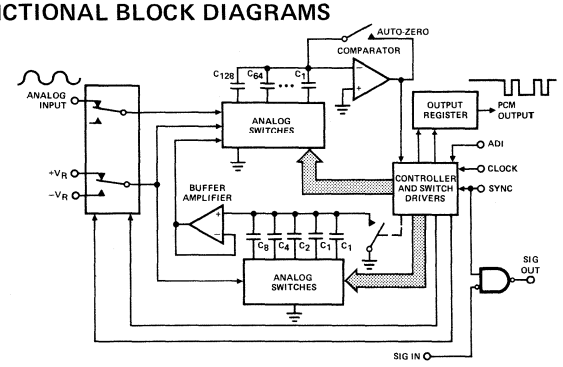
- **Minimizes System Power Requirements**
  - Low Standby Power (11 mW Typ)
  - Typical Power 80 mW (for Pair)
- **Open Drain Digital Output Allows Easy Interface to TTL and CMOS Multiplexers**
- **Decoder Contains On-Board Sample and Hold Output**
- **Separate Analog and Digital Grounding Pins Reduce System Noise Problems**
- **Additional Digital Format Available**
  - ADI (Alternate Digit Inversion) for CCITT or Sign and Magnitude Format
- **Encoder Comparator Auto Zero Minimizes Offset Voltage**
- **Extended Bandwidth or Higher Clock Rates Compatible**
  - 3.5 KHz to 7 KHz Bandwidth Possible With 1.6 MHz to 3.0 MHz Clock

DESCRIPTION

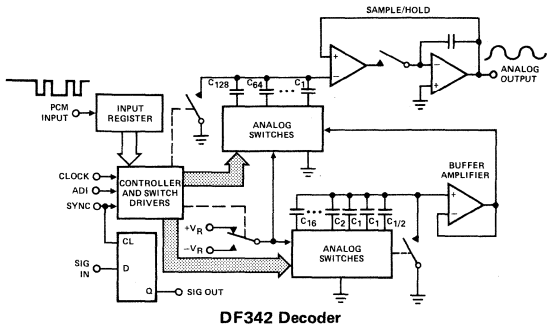
This pair of parts form a CODEC (coder-decoder set) which is designed to meet the needs of the telecommunications industry for per channel voice frequency CODECs used in PCM Channel Bank and PBX systems. The DF341 (encoder) is an analog-to-digital converter which has a transfer characteristic conforming to the telecommunication industry CCITT A-law. Its counterpart, the DF342 (decoder) is a digital-to-analog converter which also conforms to the A-law.

The pair of devices are fabricated with CMOS technology for low power. Digital output and input of the coder and decoder is in serial format. Actual transmission and reception of 8-bit data words containing the analog information is done at a 2.048 megabit/sec rate with analog signal sampling occurring at an 8 KHz rate. A sync pulse input is provided for synchronizing transmission and reception of multi-channel information being multiplexed over a single transmission line. The devices have TTL logic input levels of 0.6 V and 3.4 V that are compatible with TTL logic using a pullup resistor to +5 V; they directly interface to CMOS logic.

FUNCTIONAL BLOCK DIAGRAMS



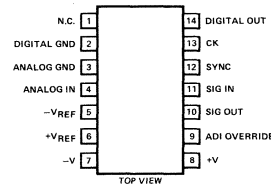
DF341 Encoder



DF342 Decoder

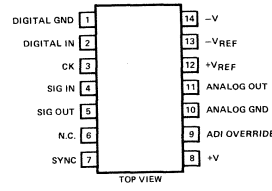
PIN CONFIGURATIONS

Dual In-Line Package



PLASTIC DIP
ORDER NUMBER: DF341CJ
SEE PACKAGE 7
CERAMIC DIP
ORDER NUMBER: DF341CP
SEE PACKAGE 11

Dual In-Line Package



PLASTIC DIP
ORDER NUMBER: DF342CJ
SEE PACKAGE 7
CERAMIC DIP
ORDER NUMBER: DF342CP
SEE PACKAGE 11

ABSOLUTE MAXIMUM RATINGS

V_{in} (Digital Inputs) . . . . . $-0.3\ V, \leq V_{in} \leq +V + 0.3\ V$
V_{in} (Analog Inputs) . . . . $-V - 0.3\ V, \leq V_{in} \leq +V + 0.3\ V$
$+V$ . . . . . $0 \leq +V \leq 11\ V$
$-V$ . . . . . $-11\ V \leq -V \leq 0$
$+V_{ref}$ . . . . . $-V \leq +V_{ref} \leq +V$
$-V_{ref}$ . . . . . $-V \leq -V_{ref} \leq +V$

V_O (Digital Output) DF341, DF342 $-0.3\ V \leq V_O \leq 15\ V$
Operating Temperature . . . . . 0 to 70°C
Storage Temperature . . . . . −55 to +125°C
Power Dissipation . . . . . 450 mW
Derate 6.5 mW/°C above 25°C

Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters to assure conformance with specs.

		Characteristic			T_A = 25°C Min	Typ Note 1	Max	Unit	Test Conditions, See Note 2: Clock = 2.048 MHz, Sync = 8 KHz Sample Rate, R_L = 820 Ω, C_L = 12.5 pF, +V = +7.5 V, −V = −7.5 V, $+V_{ref}$ = 3.0 V, $-V_{ref}$ = −3.0 V
DC Characteristics DF341 (Coder)									
1	INPUTS	I_{in} (Analog)	Analog Input Current			0.5		mA	See Note 3
2		I_{inL} (Digital)	Logic Low Input Current	Clock, Sync, Sig In, ADI Override		−0.1	−100	nA	V_{in} = 0 V; Note 4
3		I_{inH} (Digital)	Logic High Input Current			+0.1	+100		V_{in} = 7.5 V
4		C_{in} (Digital)	Logic Input Capacitance			3		pF	
5		R_{in} (Analog)	Analog Input Series Resistance			1		KΩ	Present During Sampling Time Only
6		C_{in} (Analog)	Analog Input Capacitance to Gnd			200		pF	
7		V_{in}	Dynamic Analog Input Range		$-V_{ref}$		$+V_{ref}$	V	
8		$\lvert V_{offset} \rvert$	Analog Input Offset Voltage Mag.			5	10	mV	
9	OUTPUT	C_O (Digital)	Digital Output Capacitance	Output, Sig Out		3		pF	
10		V_{OL}	Digital Output Low Voltage	Digital Output		0.3	0.5	V	I_{OL} = 3 mA
11		V_{OL}	Digital Output Low Voltage	Sig Out		0.3	0.5		I_{OL} = 1.5 mA
12		I_{OH}	Digital Output High Leakage	Output, Sig Out		0.01	10	μA	V_{OH} = 12 V
13	SUPPLY	I^+	Positive Supply Current			2.5	6	mA	
14		I^-	Negative Supply Current			−2	−6		
15		I^+_{stdby}	Standby Positive Supply Current			0.6			Analog Ground (Pin 3) Open
16		I^-_{stdby}	Standby Negative Supply Current			−0.05			
17			Supply Tolerance			±10		%	
18		I_{ref}^+	Positive Reference Current			3.5		μA	See Note 3
19		I_{ref}^-	Negative Reference Current			−3.5			
AC Characteristics DF341 (Coder)									
20	DYNAMIC	$t_{d(on)}$	Digital Output to Sync Delay Time			80	130	ns	See Figure 2
21		$t_{d(off)}$	Digital Output to Sync Delay Time			170	220		
22		t_{dbr}	Digital Output to Clock Delay Time			65	130		
23		t_{dbf}	Digital Output to Clock Delay Time			65	130		
24		t_{fo}	Digital Output Fall Time			65	130		C_L = 100 pF
25		t_{ro}	Digital Output Rise Time			175	250		
26		t_d	Signal Output Delay from Sync				100		See Figure 4
27		t_{conv}	Complete A/D Conversion (Sampling, Data Storage, Reseting)				223	clocks	

ELECTRICAL CHARACTERISTICS (cont'd)

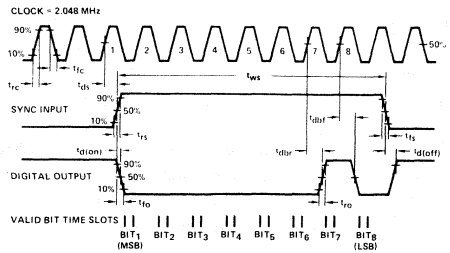
		Characteristic			T_A = 25°C Min	Typ Note 1	Max	Unit	Test Conditions, See Note 2 +V = 7.5 V, −V = −7.5 V, $+V_{ref}$ = 3.0 V, V_{ref} = −3.0 V, Clock = 2.048 MHz, Sync = 8 KHz Sample Rate	
DC Characteristics DF342 (Decoder)										
1	IN	I_{inL} (Digital)	Logic Input Current	Clock, Sync, Sig In, Dig In, ADI Override		−0.1	100	nA	V_{in} = 0	Note 4
2	IN	I_{inH} (Digital)	Logic Input Current			+0.1	+100		V_{in} = 7.5 V	
3	IN	C_{in} (Digital)	Logic Input Capacitance			3		pF		
4	OUTPUT	R_O (Analog)	Analog Output Series Resistance			50	150	Ω		
5	OUTPUT	V_{offset}	Analog Output Offset Voltage Magnitude			50	100	mV	See Note 5	
6	OUTPUT	C_L (Analog)	Analog Output Load Capacitance				100	pF		
7	OUTPUT	I_{OH}	Digital Signal Output Leakage			0.01	10	μA	V_{OH} = 12 V	
8	OUTPUT	V_{OL}	Digital Signal Output Voltage			0.3	0.5	V	I_{OL} = 1.5 mA	
9	SUPPLY	I^+	Positive Supply Current			3.5	6	mA		
10	SUPPLY	I^-	Negative Supply Current			−2.5	−6			
11	SUPPLY	I^+_{stdby}	Standby Positive Supply Current			0.8			Analog Ground (Pin 10) Open	
12	SUPPLY	I^-_{stdby}	Standby Negative Supply Current			0.07				
13	SUPPLY		Supply Tolerance			±10		%		
14	SUPPLY	I_{ref}^+	Positive Reference Current			3.5		μA	See Note 3	
15	SUPPLY	I_{ref}^-	Negative Reference Current			−3.5				
AC Characteristics DF342 (Decoder)										
16	DYNAMIC	t'_{ds}	Sync to Clock Delay Time		−100		100	ns	See Figure 3	
17	DYNAMIC	t'_{sd}	Data to Clock Setup Time		100					
18	DYNAMIC	t'_{dh}	Data to Clock Hold Time		100					
19	DYNAMIC	t'_{ss}	Signal Input to Sync Setup Time		100				See Figure 5	
20	DYNAMIC	t'_{sh}	Signal Input to Sync Hold Time		100					
21	DYNAMIC	t'_d	Signal Output to Sync Delay Time				1000			
22	DYNAMIC	t'_{do}	Analog Output Delay Time				15	μsec	See Figure 3	
23	DYNAMIC	Slew+	−3 V to +3 V Analog Output Slew			5		V/μs	C_L = 100 pF	
24	DYNAMIC	Slew	+3 V to −3 V Analog Output Slew			5				
25	DYNAMIC	Droop	Analog Output Droop Rate			0.01		%/μs		
26	DYNAMIC	t'_{conv}	Complete D/A Conversion (from Data Input to Analog Output and Internal Resetting)				52	clocks		
System Characteristics, Per Individual Part: DF341, DF342										
27		S/D	Signal to Distortion: Total of Quantizing Noise, Thermal Noise and Harmonic Distortion with Sinusoidal Input and Flat Response Filter (0.3 KHz to 3.4 KHz Bandwidth) See Note 6		34	37		dB	P_{in} = 0 to −30 dBmO	f_{in} = 1020 Hz
28		S/D			29	32			P_{in} = −40 dBmO	
29		S/D			24	27			P_{in} = −45 dBmO	
30		G_T	Gain Tracking: Method 1) Deviation of Gain from −10 dBmO Level. White Noise Source Signal Input		−0.25	±0.15	+0.25		P_{in} = −10 to −55 dBmO	
31		G_T			−0.5	±0.25	+0.5		P_{in} = −55 to −60 dBmO	
32		G_T	Gain Tracking: Method 2) Deviation of Gain from −10 dBmO Level. Sinusoidal Signal Input		−0.25	±0.15	+0.25		P_{in} = +3 to −40 dBmO	f_{in} = 1020 Hz
33		G_T			−0.5	±0.15	+0.5		P_{in} = −40 to −50 dBmO	
34		G_T			−1.5	±0.25	+1.5		P_{in} = −50 to −55 dBmO	
35		N_{IC}	Idle Channel Noise: Coder (DF341) to Decoder (DF342) of Known Quiet Code Output			−75	−72	dBmOp	V_{in} = 0 V	
36		N_{QC}	Quiet Code Output: Output of Decoder (DF342) for +0 V Equivalent Digital Code			−80	−78		Digital Input = All Zeros (using "ADI Override" = HI)	

NOTES:

1. Typical values are for Design Aid only and not subject to production testing.
2. $V_{in} \geq$ 3.4 V for logic "1", $V_{in} \leq$ 0.6 V for logic "0" for logic input levels.
3. Peak currents of up to 2 mA occur during reconstruction of Analog Output and during encoding of Analog Input.
4. Leakage testing is done at +7.5 V and 0 V to assure test at worst case conditions. Normal logic levels are described in Note 2.
5. Use of a load resistance ≥ 10K Ω is recommended to avoid output attenuation.
6. Specifications are for pair (coder and decoder).

DF341 ICBR
DF342 ICBS

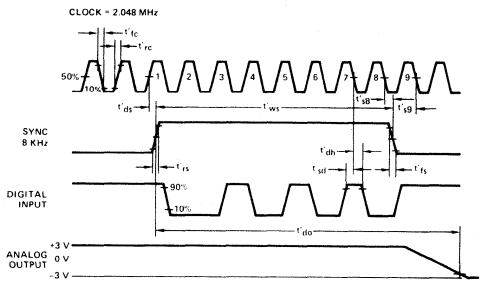
SWITCHING AND LOGIC WAVEFORMS



DF341 Encoder Waveforms
Figure 2A

Parameter		Test Condition	Min	Max	Unit
t_{ds}	Sync to Clock Delay			±100	ns
t_{rc}	Clock Rise Time	50		100	
t_{fc}	Clock Fall Time	50		80	
t_{rs}	Sync Rise Time	50		100	
t_{fs}	Sync Fall Time	50		100	
t_{ws}	Sync Pulse Width	3.906	8/F_{CLOCK}		µs
t_{ps}	Sync Pulse Period	125			

DF341 Encoder Waveforms
Figure 2B

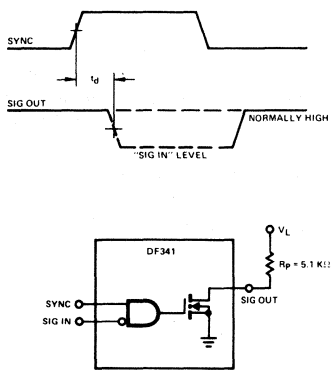


DF342 Decoder Waveforms
Figure 3A

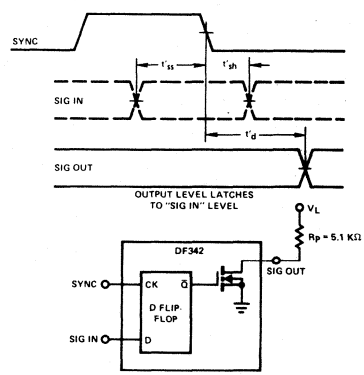
Parameter		Test Condition	Min	Max	Unit
t'_{rc}	Clock Rise Time	50		100	ns
t'_{fc}	Clock Fall Time	50		80	
t'_{rs}	Sync Rise Time	50		100	
t'_{fs}	Sync Fall Time	50		100	
t'_{s8}	Clock 8 Fall Time to Sync Fall Time		50		
t'_{s9}	Sync Fall Time to Clock 9 Fall Time		50		
t'_{ws}	Sync Pulse Width	3.906	*	*	µs
t'_{ps}	Sync Pulse Period	125			

*Minimum sync pulse width determined by 50 ns min for t'_{s8}.
Maximum sync pulse width determined by 50 ns min for t'_{s9}.

DF342 Decoder Waveforms
Figure 3B



Encoder DF341 Signal Logic Waveform
Figure 4



Decoder DF342 Signal Logic Waveform
Figure 5

FUNCTIONAL DESCRIPTION

Analog Input (Encoder DF341): The analog input voltage is sampled through a 1 KΩ resistance switch to a 200 pF capacitor array for A-D conversion. The capacitor array stores the sampled voltage for conversion. This input must be bandlimited to less than 1/2 the CODEC sample rate and have peak voltage signals less than the value of the reference voltages to achieve correct conversion.

Digital Output (Encoder DF341): The digital output of the encoder is an 8-bit serial bit stream digital representation of the analog input. The bit format is dependent on the state of the "ADI Override" pin. The serial bits are shifted out when the sync pulse goes high, occurring at each positive transition of the CLOCK (see Figure 2, Encoder Waveforms). The open drain N-channel output driver allows easy wire-OR multiplexing with other encoder outputs.

Clock Input (Encoder and Decoder): The clock input accepts a clocking signal to provide clocking of the internal logic and also sets the data transmission rate for the CODEC. Typical clock rate is 2.048 MHz with a maximum of 3.0 MHz. Refer to applications section for discussion of clock rates versus sampling rates. The clock input is internally buffered, providing quasi-TTL compatible logic levels of 0.6 V and 3.4 V. Refer to "Logic Compatibility" for details.

Sync Input (Encoder and Decoder): The sync input accepts a sync pulse for strobing of either encoder or decoder shift registers. The quasi-TTL compatible buffered input (refer to "Logic Compatibility" for details) requires an 8-clock wide sync pulse (typically 3.9 μsec wide). The sampling rate of the conversions are set by the sync pulse period (typically 8 KHz or 256 clocks). Refer to applications section for discussion of sample rates versus clock rates. The sync pulse enables the encoder output to serially shift its digital data out at the clock rate. The decoder digital input shift register accepts the data input when the sync pulse is high, shifting data in with the clock. The restrictions shown in Figure 3 Decoder Waveforms (t'_{s8}, t'_{s9}) are to insure the sync pulse is still high while shifting in the 8th bit, and the sync pulse is low before the shift register can erroneously load a 9th bit. The sync input is also used as a gating/clocking function for the "signal logic" included on each chip.

Digital Input (Decoder DF342): The digital input will shift the 8-bit serial data into its shift register upon receipt of the sync pulse. The data is loaded through a buffered input (refer to "Logic Compatibility" for details) for quasi-TTL compatibility. The shift register samples the data beginning at the positive clock transition, and shifts the data into the latch at the negative clock transition. Refer to Figure 3 Decoder Waveforms for requirements on digital input settling and data hold times.

Logic Compatibility (Encoder and Decoder): To provide more versatile logic compatibility in various systems—the chips have a logic buffer to provide logic input levels of 0.6 V and 3.4 V for the sync, clock, signal inputs and decoder digital input. This allows compatibility with TTL logic using a pullup resistor to +5 V. The levels allow direct interface to CMOS, powered by +5 V to +7.5 V.

The logic outputs are compatible with TTL or CMOS because of an open drain N-channel MOS output. The output is tied with a pullup resistor to the power supply (+5 V to +12 V) of the logic family being used.

Analog Output (Decoder DF342): The analog output is a sample and hold buffer, giving a stairstep voltage output, each voltage step has a width of the sync period (which is the inverse of the sample rate). The voltage level is the amplitude of the signal sample taken at the encoder analog input, thus the companding A/D, D/A conversions yield a linear overall transfer function (analog input to analog output).

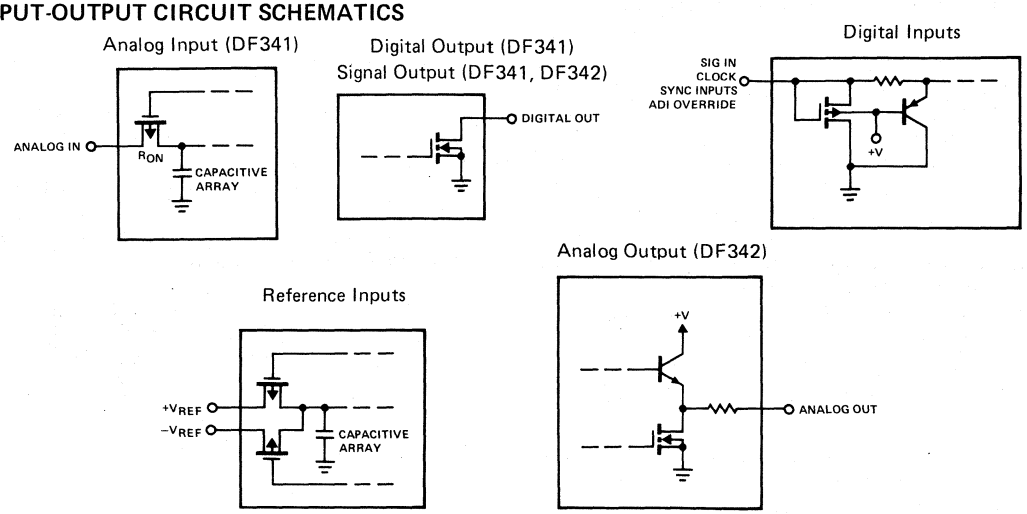
Reference Voltage Inputs (Encoder and Decoder): Positive and negative DC reference voltages are required for both encoding and decoding, and to obtain the best signal-to-distortion system performance they should track each other to 1%. The normal reference levels of ±3.0 V set the maximum analog signal swing.

Signal Logic (Encoder DF341): A signal logic gate is provided to put signal information on a separate data line. This signal input is TTL compatible and is gated to the signal output by the sync pulse being high. Referring to Figure 4, the open drain N-channel MOS is normally off; when the sync pulse goes high, the "signal input" level is transferred to the signal output.

Signal Logic (Decoder DF342). On the decoder, a D flip-flop is provided for the signal logic, giving a constant output for the strobed data. The signal input can be a common data line for signalling, the sync pulse strobing the flip-flop to sample the logic level and transfer it to the open drain N-channel MOS output. The signal input is TTL compatible (refer to "Logic Compatibility" for details).

ADI Override (Encoder and Decoder): This A-law CODEC contains the logic necessary to format the data in the CCITT Alternate Digit Inversion (ADI) pattern. The internal digital format is in sign (positive ≡ 1) plus magnitude structure. The encoder digital output format and decoder digital input format can be switched by the "ADI Override" pin between CCITT ADI format, or sign plus magnitude. For the "ADI Override" tied to ground or left open, the digital format is CCITT ADI (with the sign MSB = bit no. 1, *even* bits are inverted). With "ADI Override" tied to the positive 7.5 V power supply the output format is sign plus magnitude.

INPUT-OUTPUT CIRCUIT SCHEMATICS

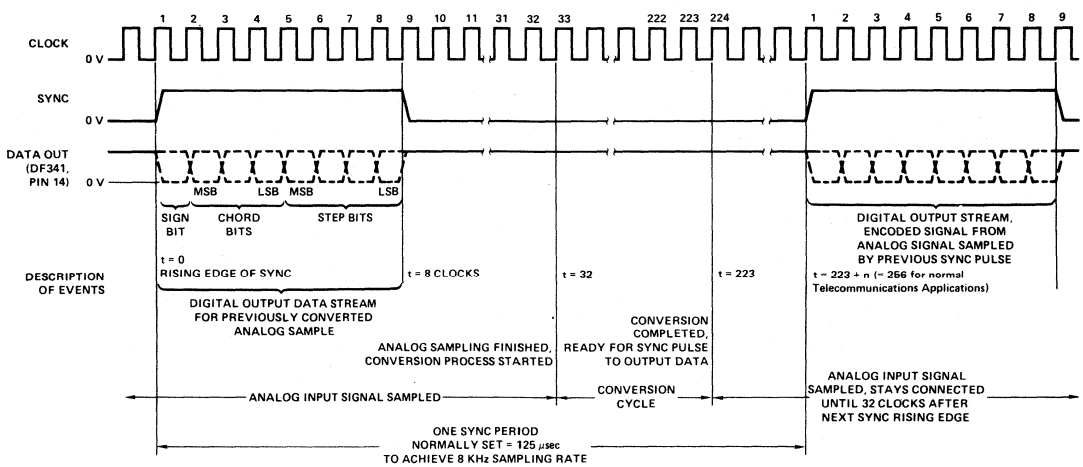


APPLICATIONS INFORMATION

The positive and negative voltage references should be bypassed to analog ground with a 10 μF capacitor to supply the peak currents required (up to 2 mA) during sampling. Inadequate bypassing may cause sampling inaccuracy and crosstalk between adjacent channels. The absolute values of the positive and negative voltage references should track each other so that conversions of positive amplitude signals track conversions of negative amplitude signals. This tracking results in the best signal-to-distortion system performance. The matching of encoder references to decoder references will insure that overall gain levels of the conversions will track each other—giving best gain tracking for matching of reference values.

As discussed in the Functional Description, the digital inputs are quasi-TTL compatible (except ADI Override). The logic input levels are 0.6 V and 3.4 V, providing compatibility with TTL logic if the gates are pulled up toward the 5 V TTL supply. Direct compatibility with CMOS logic allows 5 V to 7.5 V CMOS logic circuits to be used with the CODECs.

The sample rate of the CODEC is determined by the clock rate and the period between sync pulses. The minimum period allowed between sync pulses is 223 clock periods for the encoder, this time is required by internal logic for the encoder to complete an analog-to-digital conversion (Figure 6). For the decoder, 52 clock periods are needed as minimum time between decode sync pulses to allow complete conversion and internal resetting. For a functional system, the maximum clock rate is 3.0 MHz. The sampling of the system occurs at every sync pulse—thus the sample rate is the inverse of the sync period.



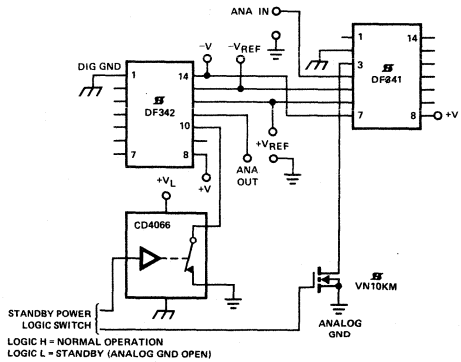
CODEC Timing Relationships
Figure 6

APPLICATIONS INFORMATION (cont'd)

The relationship between the number of clock pulses needed for conversion and clock rates puts restrictions on min or max sampling rates. For an 8 KHz sample rate, with the required minimum 223 clocks between samples, the minimum clock frequency is 1.783 MHz. At 3.0 MHz (maximum clock frequency) the maximum sample rate (with minimum 223 clocks between samples) is 13.45 KHz. For the decoder, with its minimum clocks between conversions of 52, a higher sample rate is possible. A single decoder can operate at a high sampling rate for increased bandwidth, with digital data coming from multiple encoders, operating at a slower (but staggered) sample rate. For a 2.048 MHz clock, the maximum decoder sample rate is 39.38 KHz, allowing up to 4 encoders (operating each at their max sample rate of 9.18 KHz) to go to one decoder.

Proper PC board layout techniques are required to obtain best analog system performance. Signal-to-distortion and idle-channel noise are affected by the layout of clock and sync lines relative to analog inputs and outputs, analog ground, and references. The analog ground should be kept separated from the digital ground until connected together back at the supply to avoid ground loop noise voltage on the analog ground. Bypassing of the references are recommended to analog ground to avoid superimposing digital ground noise on the reference voltage.

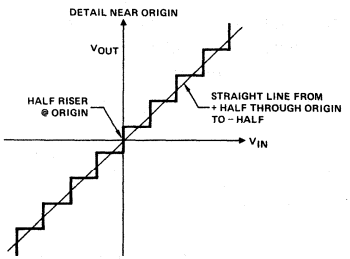
The CODECs can be put into a lower power standby condition. For standby, analog ground lines are open circuited. Relays or FET switches can be used. Figure 7 shows one implementation for standby switching. For the encoder (DF341) the switch must be low $R_{DS(ON)}$ (<25 Ω) and have very low total offset voltage (<5 mV at 200 μA current). The VMOS switch shown (VN10KM) achieves these requirements. The decoder is not as critical, offset voltage should be minimized (<50 mV); use of a CD4066 CMOS switch is satisfactory.



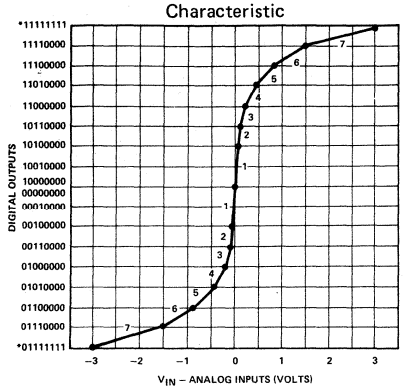
Coder/Decoder Circuit with Switches for Standby Power Condition
Figure 7

SUMMARY – CLOCK RATE/SAMPLE RATE RESTRICTIONS			
		Encoder DF341	Decoder DF342
	Min. # of Clocks for Conversion	223 Clocks	52 Clocks
Maximum Sample Rate For:	2.048 MHz Clock	9.18 KHz	39.38 KHz
	3.0 MHz Clock	13.45 KHz	57.69 KHz
Minimum Clock Freq For:	8 KHz Sample Rate	1.784 MHz	416 KHz
	4 KHz Sample Rate	892 KHz	208 KHz

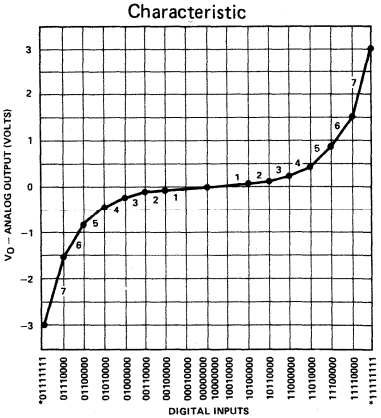
Transfer Curve Linearity – Coder/Decoder
DF341, DF342



DF341 A-Law Coder Transfer Characteristic



DF342 A-Law Decoder Transfer Characteristic



*THESE CODES ARE THE LAST STEP IN THE 7TH CHORD THAT ALSO REPRESENTS THE OVERRANGE CODE.
CODES SHOWN ARE FOR 1ST STEP AT BEGINNING OF EACH CHORD IN SIGN + MAGNITUDE FORMAT, WITH ADI OVERRIDE HI (PIN 9).
THE ACTUAL TRANSMISSION USING CCITT ADI (PIN 9 LOW) CONSISTS OF EVEN BITS INVERTED 2, 4, 6, 8. FOR EXAMPLE: THE POSITIVE OVERRANGE VALUE, 11111111 IS TRANSMITTED 10101010.

Siliconix

Function/Application of the DF331/332 New Companding Converter Chip Set

Thomas J. Mroz

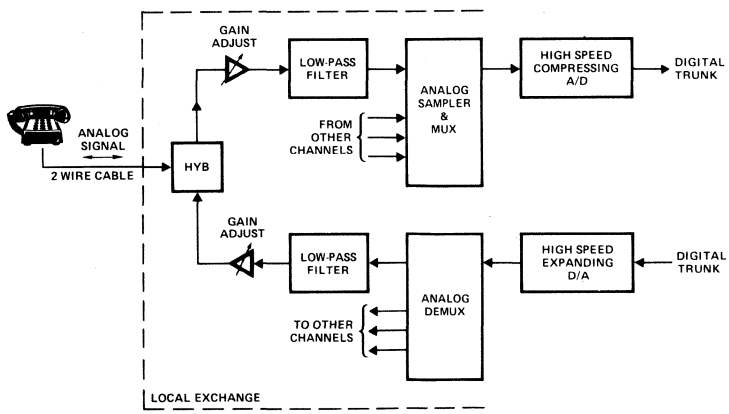
INTRODUCTION

The DF331/332 CODEC (coder/decoder) chip set offers the telecommunications industry an alternative in classical channel bank designs and a spectrum of application solutions outside of telecommunications.

Being the first commercially produced CMOS A/D, D/A converters to use a conversion technique incorporating a binary weighted capacitive array, the DF331/332 offer low power consumption, 12-bit resolution about zero and 72 dB dynamic range.

Telecommunications

Historically, the approach to doing the A/D and D/A conversion of the analog voice signals was as shown in Figure 1. This approach required the use of a high speed coder and decoder sampling at a 24 x 8 KHz rate for a 24 channel system. Because of analog multiplexing and demultiplexing this system was susceptible to crosstalk problems. Introduction of the Siliconix DF331/332 converters offers the channel bank designer an alternative system which replaces the high speed, high cost converters previously required with a low speed, low cost, high performance per channel LSI circuit. In this new system (Figure 2), each line of analog voice is individually coded or decoded by a dedicated converter. Multiplexing is now done after coding and demultiplexing on the receiving end is done prior to the D/A conversion. This approach virtually eliminates crosstalk between adjacent channels. Filter type, positioning and number remains the same as in the shared converter systems.



PCM in Existing Systems
Figure 1

Coding and Decoding

The μ-255 law, which is currently is use in the U.S., defines the transfer characteristic to be used in doing the analog (voice) to digital conversion in a telecommunication channal bank. The μ-255 law itself is defined by the equation:

$$F_{|x|} = S_{gn}(x) \frac{\ln(1 + \mu |x|)}{\ln(1 + \mu)}$$

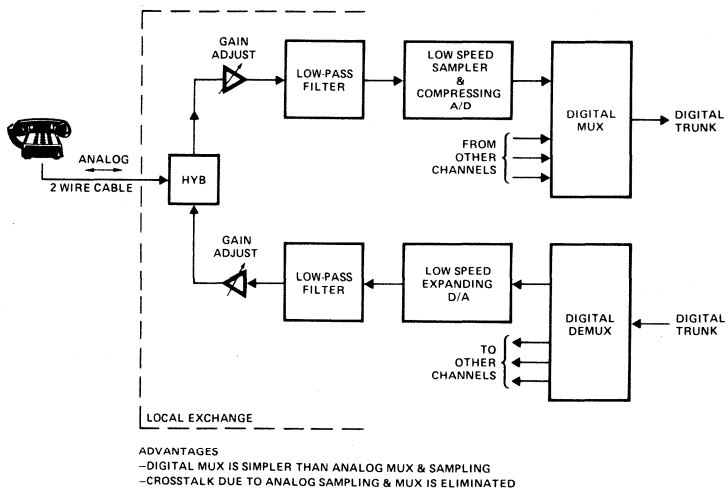
where $\mu = 255$.

Actual representation of the equation is done in a piecewise linear fashion. Thus, the transfer curve is comprised of 16 sections called chords, each of which contains 16 discrete steps (Figure 3). Decoding (Figure 4) is accomplished by implementation of the inverse transfer characteristic.

Pulse code modulation (PCM) is the method by which information is transferred between sending and receiving channel banks. The output of the A/D converter consists of an eight bit digital word which is the resultant of an analog sample. Sampling occurs at an 8 KHz rate while data transfer is done at 1.544 MHz. Maximum sampling frequency for the DF331 is 16 KHz when using a 3.088 MHz clock frequency.

Digital output of the DF331 is structured as a sign bit + magnitude (7 bits) word. Of the 7 bits following the sign the first three are dedicated to chord selection while the last four indicate which of the 16 steps within each chord contains the analog sample.

Decoding with the DF332 can be done at up to a 32 KHz rate while still using a 1.544 MHz clock.



Use of PCM with Per Channel CODEC
Figure 2

DF331 μ-Law Coder Transfer Characteristic

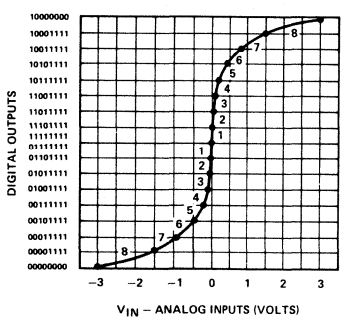


Figure 3

DF332 μ-Law Decoder Transfer Characteristic

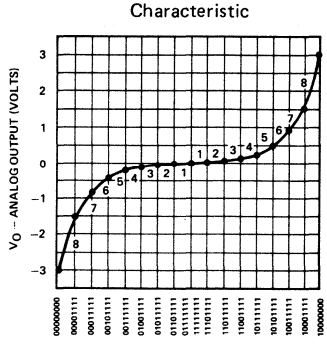


Figure 4

Non-linearity of the transfer characteristic results in a nearly constant signal to Quantizing Noise (S/Nq) ratio over a wide range of analog voice amplitudes (Figure 5). This, in telephone applications, makes possible a high degree of intelligibility when someone is speaking softly or very loudly into a phone. A linear transfer characteristic would result in a constant decay of voice quality as signal levels decreased.

A/D, D/A Conversion Algorithms

Actual conversions (A/D, D/A) are accomplished through the use of capacitive arrays on board the DF331 and DF332. For purposes of this discussion the array which is used to determine the chord in which the sample lies will be called the X-array. Steps are determined by a second array called the Y-array. The X-array contains 256 capacitors which are connected in a binary weighted fashion. The Y-array contains 16 capacitors connected in a like manner (Figure 6). Care was taken in layout to minimize edge effects which could cause mismatch between these capacitors. Top plates (metal) of all capacitors are common and are connected to one of the inputs of a comparator. The other comparator input is analog ground. Bottom plates of the capacitors of the array can be switched between V_{IN}, $+V_{REF}$, $-V_{REF}$ and ground. Principle steps in doing an A/D conversion are:

1. Acquire sample.
2. Determine sign.
3. Determine chord.
4. Determine step within the chord.
5. Load output shift register.
6. Reinitiate the system and return to sample mode.
7. Output data (digital).

During sampling the top (metal) plate of the capacitor array is connected to ground. The entire array is then charged to the input signal voltage via an analog switch. After sampling is complete, the switch grounding the top plate of the array is opened and the bottom plates of all capacitors are switched to ground. The top plate, being the input to a comparator, now has $-V_{IN}$ as a voltage. Sign of the input is determined by examining the comparator output.

Upon determination of the sign the selection of the appropriate reference is made. Chords are now selected by throwing the switches at the bottom plates of the capacitors, in a successive approximation manner, to the reference chosen while monitoring the comparator output.

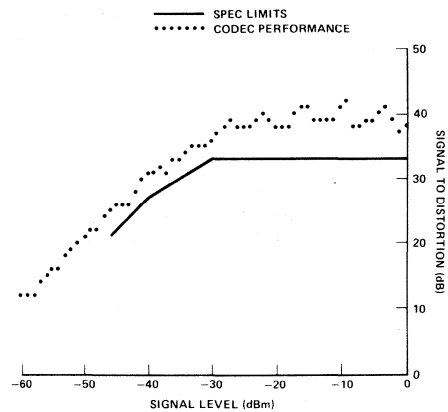
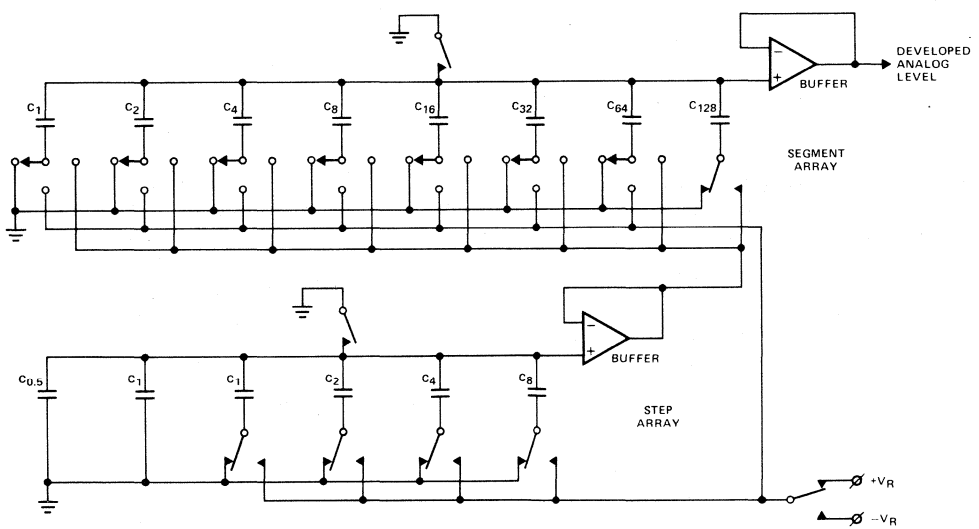


Figure 5



D to A Converter Based on Capacitive Ladders
Figure 6

During these steps the voltage at the top plate of the array is defined by the equation:

$$V_O = \frac{C_A}{C_A + C_B} \times V_r - V_{IN}$$

where C_A is the equivalent capacitance being switched to the reference and C_B is the equivalent capacitance remaining switched to ground. Since the capacitors are binary weighted C_{X8} equals 128 C_X. As an example then, if C_{X8} was switched to the reference, the comparator would see,

$$\frac{128\,C_X}{128\,C_X + 127\,C_X} \times V_r - V_{IN} \text{ or } \frac{128}{255} \times V_r - V_{IN}$$

which also indicates that the reference will be the same in polarity as the sample. The comparator output not changing after switching C_{X8} would indicate that the sample lies in the 8th chord.

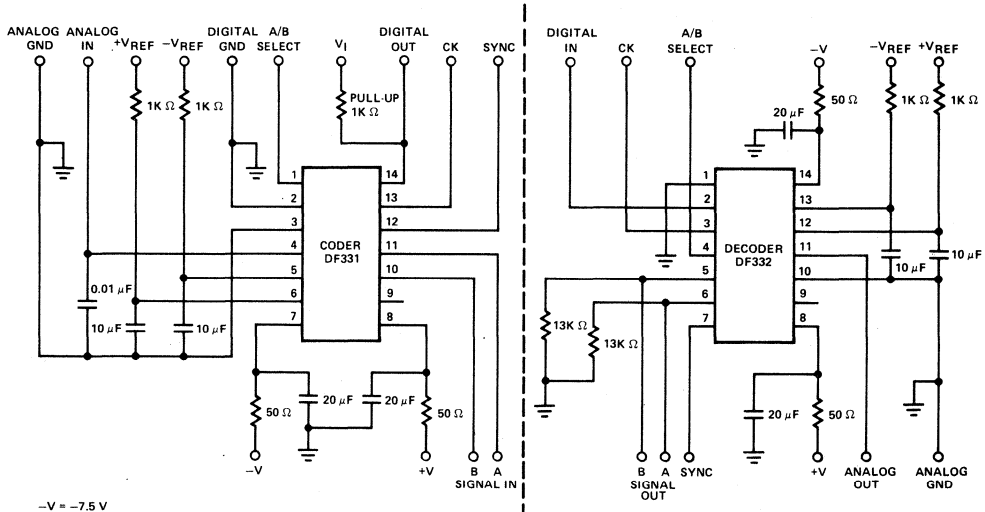
Step value is determined by switching the X-array capacitor indicating chord from the reference to the Y-array buffer output. Successive approximation techniques are again used to develop a step voltage. A fraction of this voltage, as determined by the X-array, appears at the comparator input. Transitions of the comparator output are monitored until the step value is determined.

After these determinations are made, the 8 bit binary word corresponding to the switch positions is loaded into the output shift register. The entire conversion system is then reinitiated and goes into a sampling mode.

The next sync pulse presented to the encoder transmits the previous data and starts the sequence over again.

General Considerations When Using the DF331/332

When using the DF331/332 in communication systems it is necessary to bypass certain pins to ground to reduce noise injection into the converters which could be detrimental to system performance. Figure 7 shows suggested external components to be used on a D_3 channel bank card. Important to note, is that references are bypassed to analog ground rather than digital ground. This prevents digital noise from being coupled into the reference pins. Analog ground must be connected to digital ground at some point. It's preferable that this point be at the supply or near, to prevent current flow through the analog ground, which would introduce offsets and noise at the analog input. Decoupling of coders and decoders is accomplished with the 50 Ω/20 μF networks in series with the supplies and the 1K/10 μF networks in series with the references. This circuit is typical of a D_3 channel having an 8 KHz sample rate.



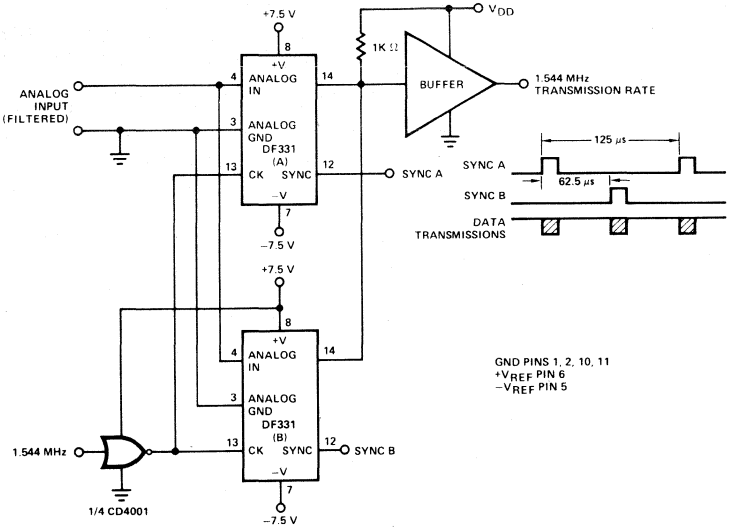
−V = −7.5 V
+V = +7.5 V
$-V_{REF}$ = −3.0 V
$+V_{REF}$ = +3.0 V
V_I = AS REQUIRED FOR INTERFACING
CK = 1.544 MHz
SYNC = 8 kHz (PER DATA SHEET)
LOGIC LEVELS = 0–7.5 V

Transmit Section **Receive Section**

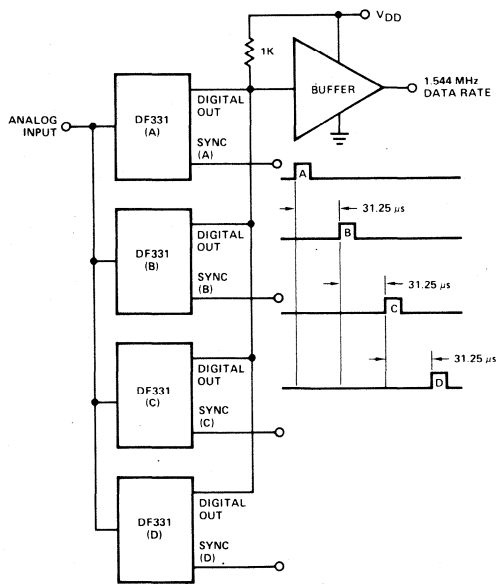
Typical D_3 Channel (Less Filters)
Figure 7

APPLICATIONS

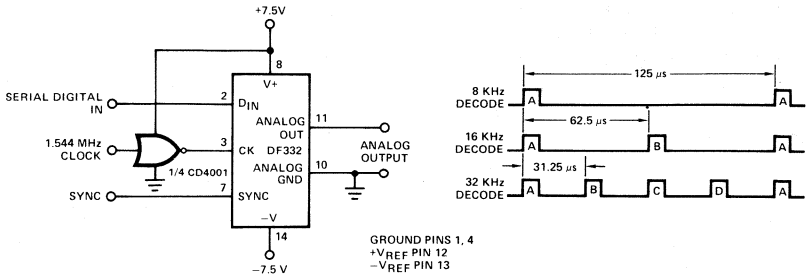
Circuits for various bandwidth requirements are shown in Figures 8, 9, 10 and 11. There exists several ways of achieving bandwidths wider than the 4 KHz required for a D_3 channel bank. Most obvious is a simple doubling of the clock frequency which allows a doubling of the sample rate. Therefore, a 3.088 MHz clock enables the use of a 16 KHz sample rate. The higher clock rate can prevent the use of CMOS in external circuitry, however, and the circuit of Figure 8 may become more economical from a power stand point. This circuit incorporates the 1.544 MHz, or slower clock rate by using multiple coders which are alternately sampling to accomplish a 16 KHz sample rate. This same technique can be expanded to perform a 32 KHz sample rate while needing only one decoder, Figure 10, to perform the D/A conversion. This is possible since decoding takes roughly a quarter of the time coding requires. Time for coding and decoding is directly related to a fixed number of clocks. Therefore, doubling of the clock frequency enables the use of a sync pulse rate twice as rapid as previously used. A minimum clock rate of around 700 KHz sets the lower limit for data transmission. No such limit exists for sample rate, however.



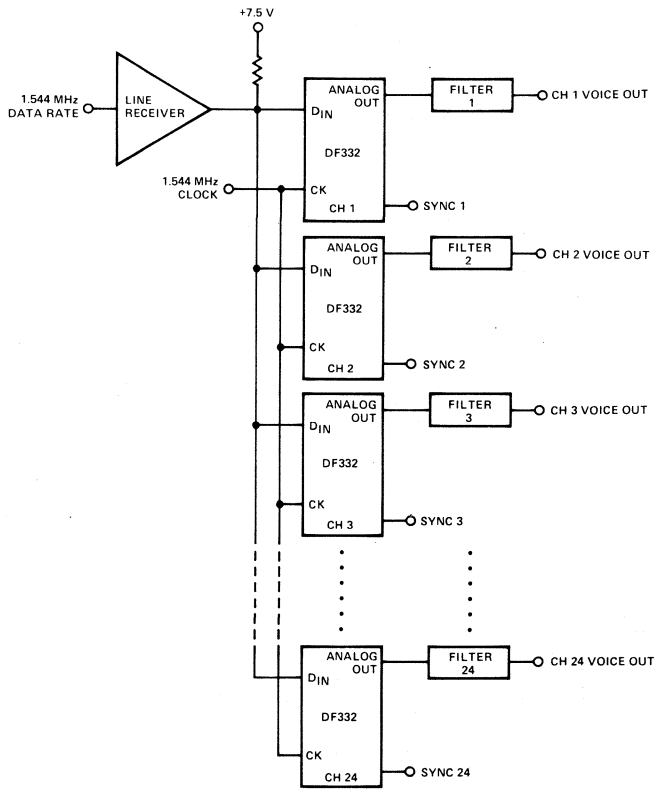
Multiple Coders for 16 kHz Sampling Rate
Figure 8



Multiple Coders for 32 kHz Sampling Rate
Figure 9



Basic Circuit for Decoding 8 KHz to 32 KHz Sampling Rate Coder Configurations Using 1.544 MHz Clock
Figure 10

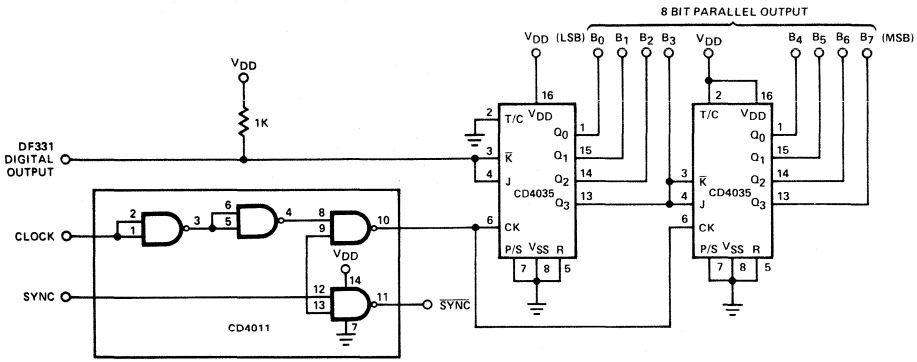


Block Diagram of a 24 Channel Decoder for D_3 Channel Banks
Figure 11

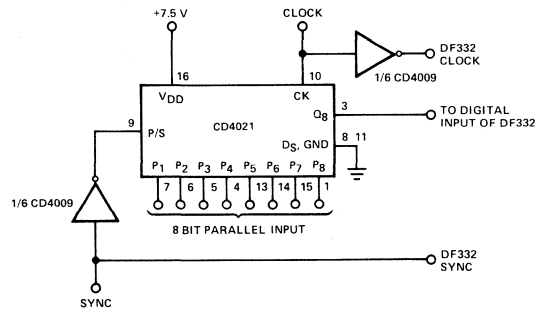
Serial to Parallel and Parallel to Serial Data Conversion

Often when interfacing external logic to the DF331/332, it may be advantageous to convert to a parallel data format after coding and to a serial format again when injecting data into the decoder. Figure 12 shows a simple 8 bit serial to parallel converter allowing easy interfacing asynchronously to systems requiring the 8 bit parallel format. During sync, data is being updated, therefore the sync output can be used as a data ready output. A single IC plus a couple of extra inverters is all that is needed to convert from parallel back to the serial format as shown in Figure 13.

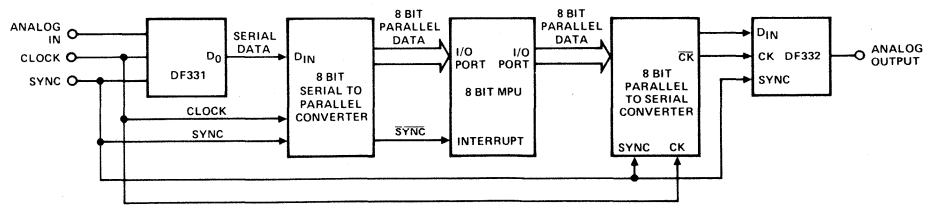
Interfacing to an 8 bit microprocessor is accomplished neatly using the previously described circuits as shown in Figure 14.



8 Bit Serial to Parallel Converter
Figure 12



8 Bit Parallel to Serial Converter
Figure 13



Typical MPU Parallel Data Interface to the DF331/332
Figure 14

Analog Demultiplexing of the Decoder

Some applications may require the use of a single decoder to decode more than one channel of information. If this is so, it is necessary to insert a dummy sync pulse between the two channel syncs to reduce crosstalk. At the time of dummy pulse the digital data should remain at all "1"s condition. Figure 15 shows the basics of such a circuit along with required waveforms.

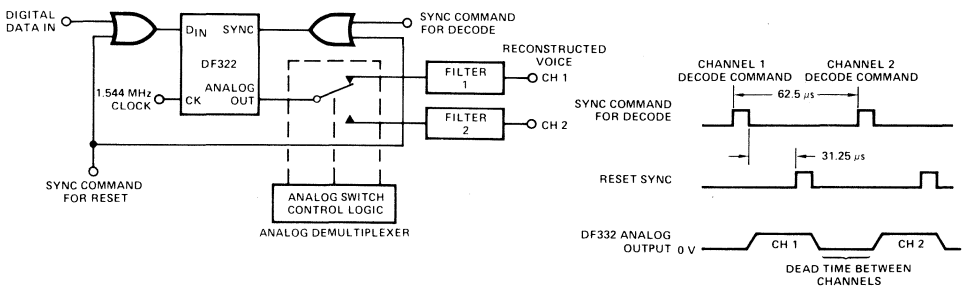
Servo Control Systems

Servo control loops offer an interesting application area in which the DF331/332 can prove useful. Since digital information is nearly immune to environmental noise, it is advantageous to convert to digital before transmitting data from a remote location to a control center. Figure 16 shows a microprocessor based servo loop and locations of the DF331/332 ICs within the loop. In this case the summer, to determine an error voltage, and the DF331 form the A to D section of the remote station. The DF332 plus integrator form the D to A conversion upon receiving data from the central control station.

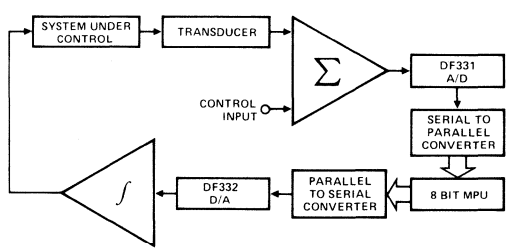
Advantages realized in a servo control loop employing the use of the DF331/332 include:

1. Digital data transmission from and to remote sites.
2. 12 bit resolution with 8 bits of data when resolving error voltages.
3. Wide dynamic range of coder and decoder allow wider breadth of feedback voltages and integrator input voltages.
4. Use of the MPU to change response characteristics of the loop based on inputs from feedback as well as external sources.

This basic configuration could prove useful in many applications where varying loop response characteristics is desirable to accommodate varying situations.



Analog Demultiplexing of the Decoder
Figure 15

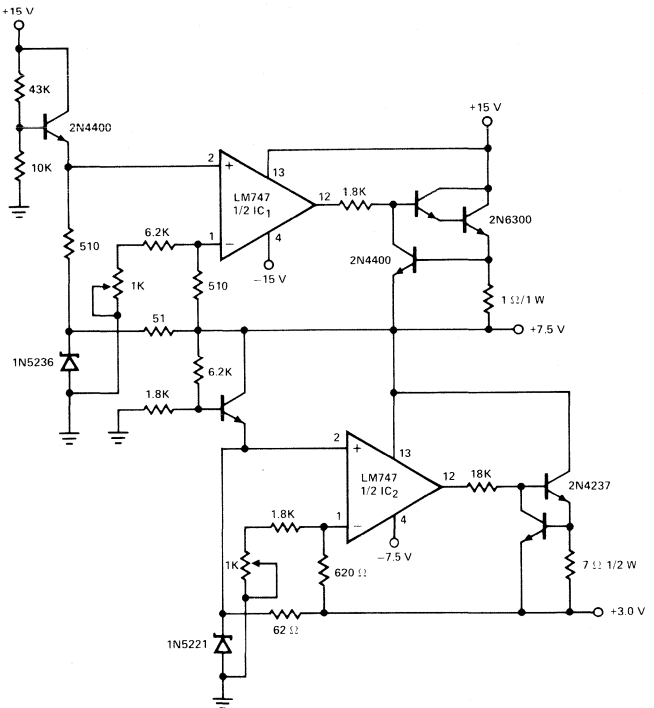


Block Diagram of a Servo Control System
Figure 16

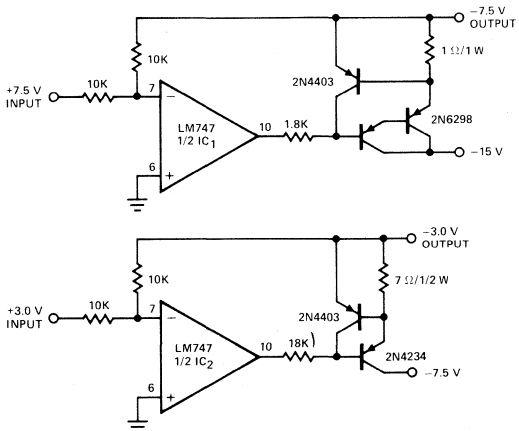
Peripheral Circuits

Circuits which may prove useful when evaluating the CODEC set are the ±7.5 V and ±3.0 V regulator circuits shown in Figures 17A and 17B. In general, the ±7.5 V supplies should be of a 10% tolerance nature. Reference supplies should be matched to one another to within 1%. Absolute value of the references and changes of the absolute values will be reflected by a gain change. The regulator shown in usable for powering 24 CODEC channels simultaneously. In most applications outside of telecommunications where signal to distortion ratio requirements are less stringent, simple three terminal regulators may be used in developing supply voltages.

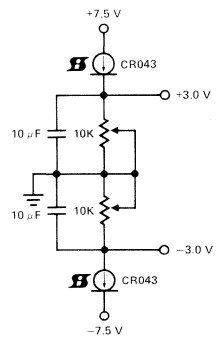
References may be supplied by using the resistor – constant current diode configuration shown in Figure 18.



Positive Supply and Reference Regulators
Figure 17A



Negative Supply and Reference Circuits
Figure 17B



±3.0 V Reference Generator
Figure 18

Sync generation can be accomplished by using the circuit in Figure 19. This is basically a divide by 24 of the clock input. The R/S flip-flop comprised of IC_2 synchronizes the sync edges to the rising edge of $\overline{CK}$. The D flip-flop following the R/S flip-flop delays the sync to the DF331 by a half clock. Thus, the proper sync/clock phase relationships are established for both coder and decoder. It is also possible to create additional sync pulses by shifting the previously generated syncs through a shift register being clocked by the system clock and $\overline{clock}$.

Offset Voltage Adjustment

Some applications may require zero input offset to be present at the coder. While the input offset of the coder is small (< 5 mV), the remaining offset can be zeroed out using the circuit of Figure 20. It is possible to inject small voltages between the analog ground and the digital ground. AC coupling the analog ground to the digital ground allows biasing of the analog ground by the 10K pot. This approach maintains analog input impedance and adds no degrading effects to the signal to be processed or the coder itself.

CONCLUSIONS

It's quite apparent that the information presented herein is generally an overview of the DF331/332. Applications not covered include audio delay lines, audio reverberation circuits, remote data acquisition and transmission and many others. The DF331/332 offers advantages over other CODEC circuits being presently manufactured by allowing system designers a new breadth in designs which reduce component count, cost and general system complexity while improving important system parameters.

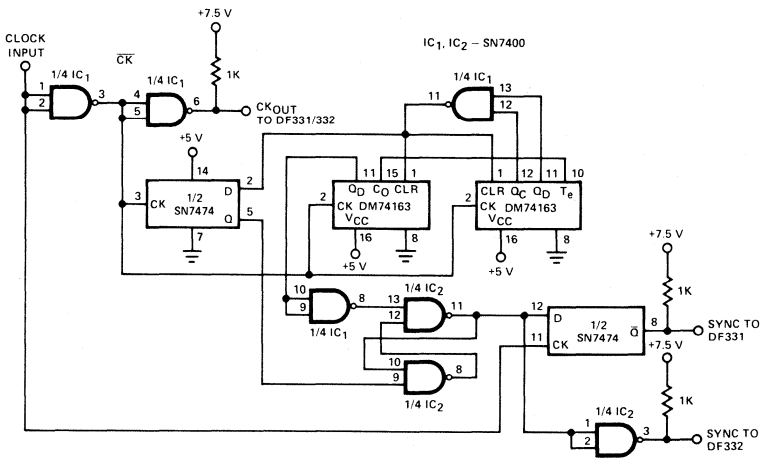
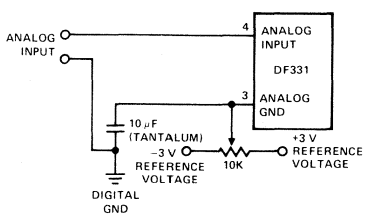


Figure 19



Analog Input Offset Adjust
Figure 20

Siliconix

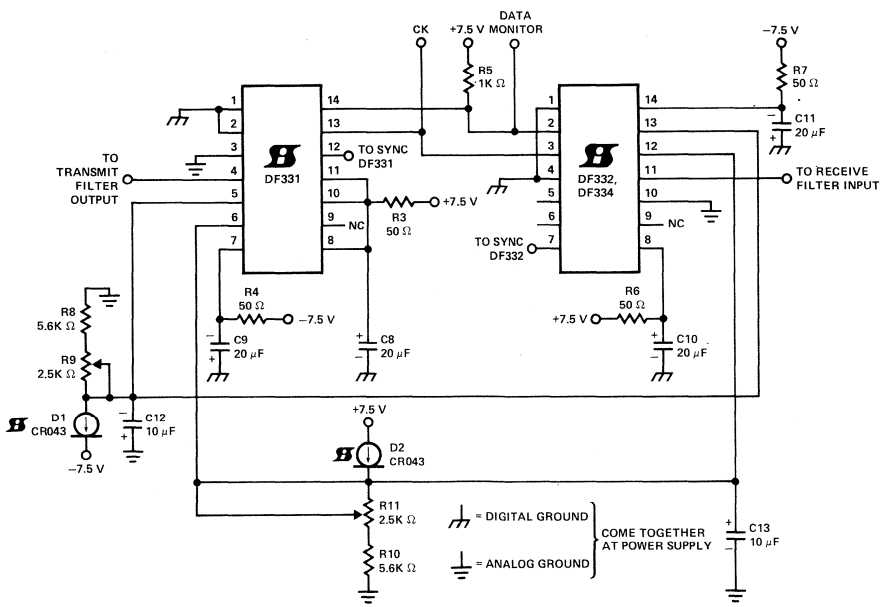
Design Aid to Build a CODEC Evaluation Demonstrator with the DF331/DF332/DF334

INTRODUCTION

The Siliconix CODEC (DF331/332) requires few external components to achieve per channel digital encoding of telephone voice signals. This design aid details the design and evaluation of a lab demonstrator for the CODEC set. Included in the demonstrator are the voltage references and the synchronization circuitry which is necessary to encode and decode a single voice channel. The encoded output of the DF331 encoder is simply applied to the digital input of the decoder. This allows an easy functional test as well as characterization of a CODEC pair.

Figure 1 shows the schematic details of the encoder and decoder with the voltage references and supply bypass elements. The ±3.0 volt voltage references are achieved by running a 430 μA current from a constant current diode (CR043) through a resistor with a trim pot for fine adjustment of the reference voltage. The references are bypassed with a 10 μF tantalum capacitor to supply the peak current (up to 2.0 mA) required by the CODEC during sampling. The digital output of the encoder (DF331), being an N-channel open drain output, requires a 1K Ω pull-up resistor.

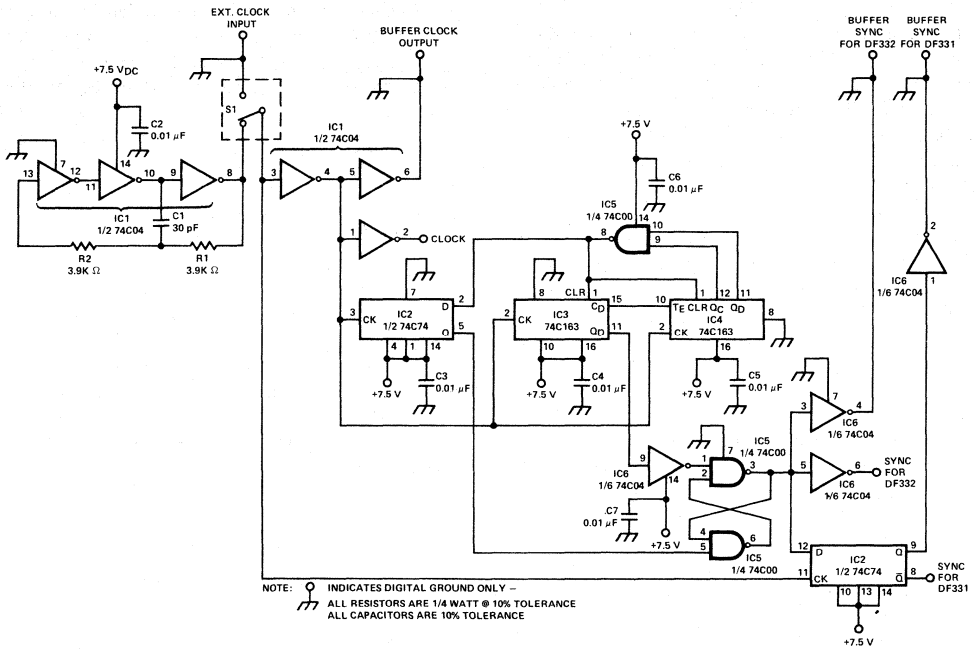
The analog and digital grounds are pinned-out separately on the CODEC, and should be tied together at the power supply ground.



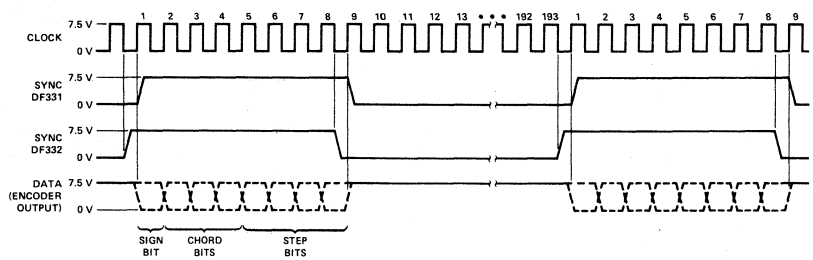
CODEC and References
Figure 1

Figure 2 shows the clock and sync generation circuitry which provides timing for the CODEC. The clock is a basic 3-gate CMOS clock with RC values set to achieve an approximately 1.5 MHz clock rate. The sync generator essentially divides the clock by 193 to provide a sync pulse which is eight clock periods wide and is applied at an 8 kHz rate. (Note that 1.544 MHz divided by 193 equals 8 kHz.) Figure 3 shows the relationship between the various waveforms generated by the sync circuitry, as well as the relationship between the sync, clock and digital data output of the encoder.

The sync waveform to the decoder (DF332 or DF334) is advanced by one-half of a clock period to allow for propagation delays which occur in the CMOS sync generator. Without advancing the DF332 sync, it is possible to lose the most significant bit in each data word, which results in a loss of the sign bit in transmission.



Clock and Sync Generator
Figure 2



Sync Generator Waveforms
Figure 3

Evaluation

This demonstrator allows simple evaluation of the CODEC set. A ±7.5 V (±10%) lab supply is applied to the CODEC and sync circuitry. Analog and digital grounds should be kept separate until meeting at the power supply ground to avoid ground loops in the analog portions of the board. Voltage references should be adjusted to ±3.0 volts. Mismatched voltage references will cause asymmetric waveforms, giving rise to harmonic distortion. References should match to within 0.1 volts.

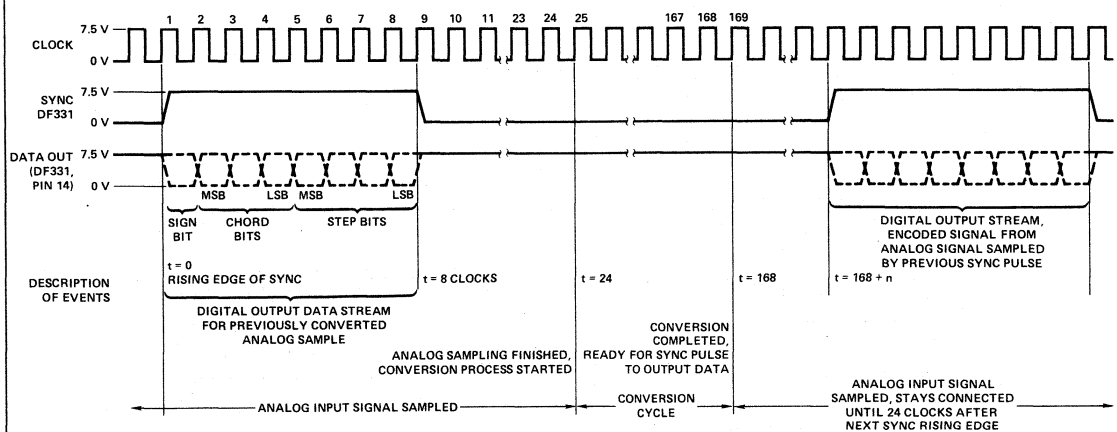
To look at the digital bit stream, the oscilloscope should be synchronized to the sync pulse of the DF331. The encoder output is seen at pin 14 of the DF331. Applying a slowly varying DC level to the analog input of the encoder allows observation of the changing data stream. The corresponding analog voltage levels should appear at the decoder (DF332) output.

For evaluation of voice or music signals, an anti-aliasing filter must precede the analog input and a filter which compensates for the sampling frequency characteristics must follow the decoder output. These filters should cut off before 4 kHz, which is one half of the sampling frequency. They are typically 5th order elliptic low pass filters.

The maximum peak signal swing through the CODEC is equal to the value of the voltage references. The CODEC will function with references as low as ±2.0 volts and as high as ±4.0 volts. Lowering the absolute value of the references compromises system dynamic range while raising the absolute value of the references increases the harmonic distortion of the system.

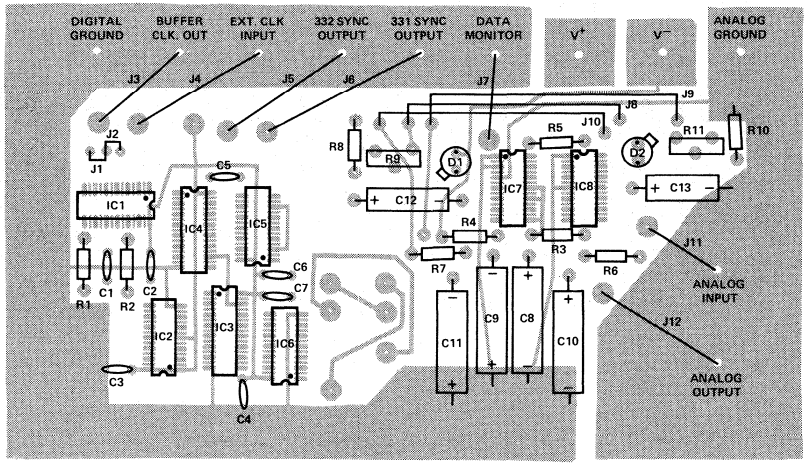
Timing of the CODEC System

The CODEC system timing is controlled by the sync pulse. Figure 4 shows the encoder (DF331) timing relationship between the sync pulse, the analog sampling time, conversion time and encoded serial digital output. As shown, the rising edge of the sync pulse starts the serial output of data, starting with the MSB of the 8 bit code (the sign bit). This rising edge of the sync pulse also starts a 24 clock countdown for sampling of the analog signal input (the sampling starts immediately after the previous conversion is completed). At the end of these 24 clocks, the analog sampling is completed and the conversion cycle begins. 168 clock pulses after the sync rising edge, the conversion will be completed and the internal registers will have the encoded data ready for output. The Encoder (DF331) will now go to the analog input sampling state until the next sync pulse. At the rising edge of the next sync pulse, the digital encoded data will be serially shifted out on the output pin. The sampling conversion process for the next analog input starts again.



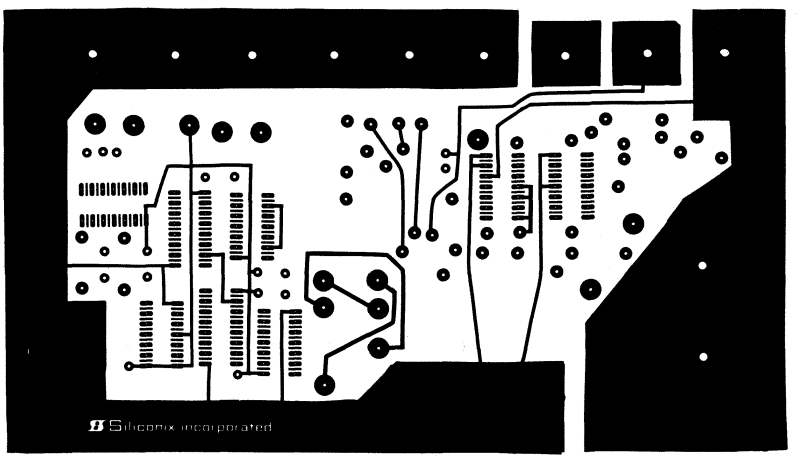
CODEC Timing Relationships
Figure 4

COMPONENT LAYOUT



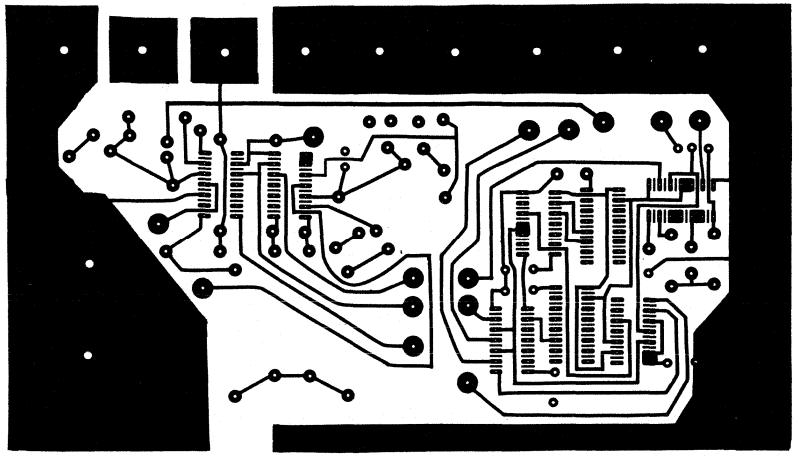
J1 CONNECTS THE INTERNAL CLOCK TO CIRCUIT
J2 CONNECTS THE EXTERNAL CLOCK TO CIRCUIT
J3 CONNECTS THE BUFFER CLOCK OUTPUT (1–6) TO BNC
J4 CONNECTS THE EXT. CLK. INPUT TO BNC
J5 CONNECTS THE 332 SYNC OUTPUT TO BNC
J6 CONNECTS THE 331 SYNC OUTPUT TO BNC
J7 CONNECTS THE DIGITAL MONITOR OUTPUT TO BNC
J8 CONNECTS R7 TO IC(8) PIN (14)
J9 CONNECTS R11 TO IC(7) PIN (6)
J10 CONNECTS R9 TO IC(8) PIN (13)
J11 CONNECTS ANALOG INPUT TO BNC
J12 CONNECTS ANALOG OUTPUT TO BNC

PC BOARD FOIL PATTERN



DF331, DF332, DF334 CODEC Demonstrator
Foil Pattern, Component Side of Board

PC BOARD FOIL PATTERN (Cont'd)



Foil Pattern, Bottom Side of Board

PARTS LIST

DEVICE	VALUE	SUGGESTED MANUFACTURER
R1, R2	3.9K Ω 1/4 Watt 5% Tolerance	Allen-Bradley
R3, R4, R6, R7	50 Ω 1/4 Watt 5% Tolerance	Allen-Bradley
R5	1K Ω 1/4 Watt 5% Tolerance	Allen-Bradley
R8, R10	5.6K Ω 1/4 Watt 5% Tolerance	Allen-Bradley
R9, R11	2.5K Ω Pot	CTS (X201 Series)
C1	30 pF Disc Mylar Capacitor	Sprague
C2–C7	0.01 μF Disc Ceramic Capacitors	Sprague
C8–C11	20 μF @ 25 WV Electrolytic Capacitor	Sprague
C12, C13	10 μF @ 25 WV Electrolytic Capacitor	Sprague
D1, D2	CR043 (Current Regulator Diode)	Siliconix
IC1, IC6	74C04 (Hex Inverter)	National
IC2	74C74 (Dual D Flip/Flop)	National
IC3, IC4	74C163 (Binary Counter)	National
IC5	74C00 (Quad NAND Gate)	National
IC7	DF331 (CODEC Encoder)	Siliconix
IC8	DF332 or DF334 (CODEC Decoder)	Siliconix
Misc.	26 Gauge Wire, BNC Connectors, IC Sockets, Non-Insulated Banana Jacks, Stand Offs, PC Board	

CONSTRUCTION HINTS

The printed circuit layout included is for a double sided board. Foil patterns are shown with the foil side facing the reader. The stuffing diagram is viewed from the component side.

OPERATION

The potentiometer R9 adjusts the negative reference voltage and R11 adjusts the positive reference voltage. Use a DVM to adjust the references to ±3.0 volts. The digital bit stream may be viewed by triggering an oscilloscope on the DF331 sync pulse and connecting the data monitor output to the scope input. The demonstrator may be clocked by an externally generated clock if desired. Connect jumper J2 (only) for external clocking; connect J1 (only) to use the internal clock.

Siliconix

Considerations for the Proper Filtering of Analog Signals in DF331/DF332/DF334 CODEC Converter Applications

Walt Heinzer

INTRODUCTION

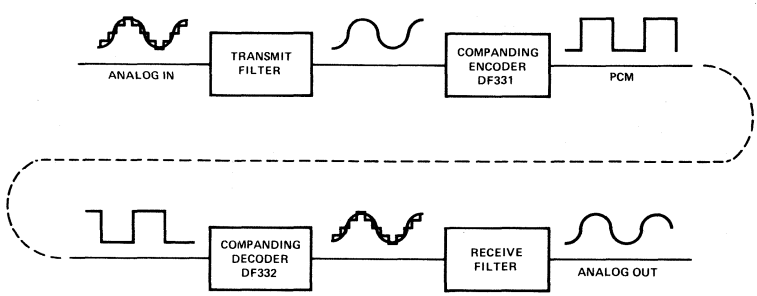
The practical use of CODEC's in telecommunications and audio systems requires two low pass filters, the transmit and receive (Figure 1). The transmit filter in telecommunications nomenclature performs the anti-aliasing (frequency folding) function. The receive* filter smooths the discrete sample voltages of the regenerated audio (voice) signal.

In order to understand the filtering requirements of the CODEC A/D–D/A system, a statement of the sampling theorem is in order:

"If a signal (voice, audio) that is bandlimited is sampled at regular intervals and at a rate at least twice the highest frequency in the band, then the samples contain all of the information of the original signal".

When the CODEC's (DF331/DF332/DF334) are used in telecommunications systems the sampling frequency (f_S) is set at 8 kHz. This implies that the maximum voice signal is limited to 4 kHz. The transmit filter is necessary to limit the input voice signal. For the 8-bit companding converter

*Sometimes called interpolation filter in telecommunications nomenclature.



Filters Used In a CODEC System
Figure 1

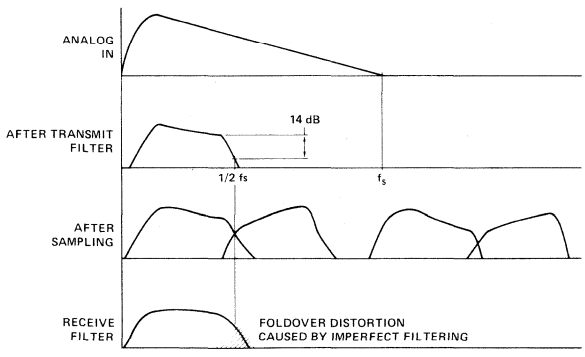
approach, 14 dB of attenuation at 1/2 the sampling frequency, reduces frequency folding (Figure 2). However, a guardband is introduced on the voice signal typically resulting in a maximum usable frequency of 3.5 kHz. The receive filter smooths the discrete voltage samples of the regenerated signal. At the same time this filter corrects the sin x/x† frequency response introduced by the CODEC sampling system back to a flat bandpass by applying an x/sin x transfer characteristic (Figure 3).

The exact specifications necessary for the transmit and receive filters are determined by the application. For the telecommunication industry the frequency and phase response characteristics are more precisely defined. D3 and D4 channel bank specifications define the overall voice-in, PCM, voice-out frequency and gain response requirements.

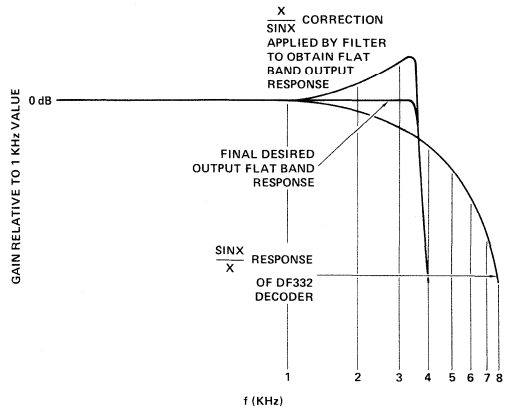
† In telecommunications f_S = 8 kHz implies $x = \frac{\pi f}{8\ \text{kHz}}$

Some of the more important specs are listed in Table I which is excerpted from "D3 Channel Bank Compatibility Specification–Issue 3" Oct. 1977 [4].

For audio and transducer applications it is important to consider sufficient filtering to avoid frequency folding and gain errors due to the sampling theorem. As a rule of thumb the passband of the transmit filter should attenuate the input signal by at least 14 dB at 1/2 the sampling frequency and by at least 30 dB at the sampling frequency. Remember that the DF331/DF332/DF334 can be operated at clock frequencies up to 3.088 MHz which results in a maximum sampling frequency (f_S) of 16 kHz. This is useful for extended bandwidth applications. The same guidelines of filter attenuation apply at this sampling frequency.



Frequency Spectrum In a Sampling System
Figure 2



Effect of Sampling Theorem on Output Gain Versus Frequency
Figure 3

Important Gain vs Frequency Requirements for Telecommunications D3 Channel Bank
Table I

FREQUENCY	TRANSMIT FILTER	RECEIVE FILTER
60 Hz	< −20 dB	N/A
200 Hz	> −3 dB	> −2 dB
300–	+0.25 dB } Passband Ripple	
3 kHz	−0.50 dB }	Same
3.4 kHz	> −1.5 dB	Same
	< 0 dB	
4 kHz	< −14 dB	Same
4.6 kHz	< −32 dB	< −28 dB

It has been shown in AN77-4 that the bandwidth can be increased by using multiple encoders (DF331's) to achieve bandwidths approaching 8 kHz ($f_{s_{eff}}$ = 16 kHz) and 16 kHz ($f_{s_{eff}}$ = 32 kHz). The filtering requirements (Figure 4) necessary to prevent fold-over are the same as the single encoder case when the new effective sampling frequency ($f_{s_{eff}}$) is used.

IMPLEMENTATION

Now that we have examined actual filter requirements–what is the correct filter implementation? There is no exact answer; however, it is worthwhile to look at a summary of some of the major filter salient features on a comparison basis.

Simple Filters (Single Pole, Double Pole)

These filters are realizable in R and C's with op amps or the traditional approach of L, R, and C's. Inductors are avoided in low frequency applications due to size, cost, and non-linearities. The frequency characteristics and example implementations are shown in Figure 5. Note that each pole contributes –20 dB/decade in roll-off between the passband and stopband. When these filters are used with the CODEC's they severely limit the usable flatband bandwidth.

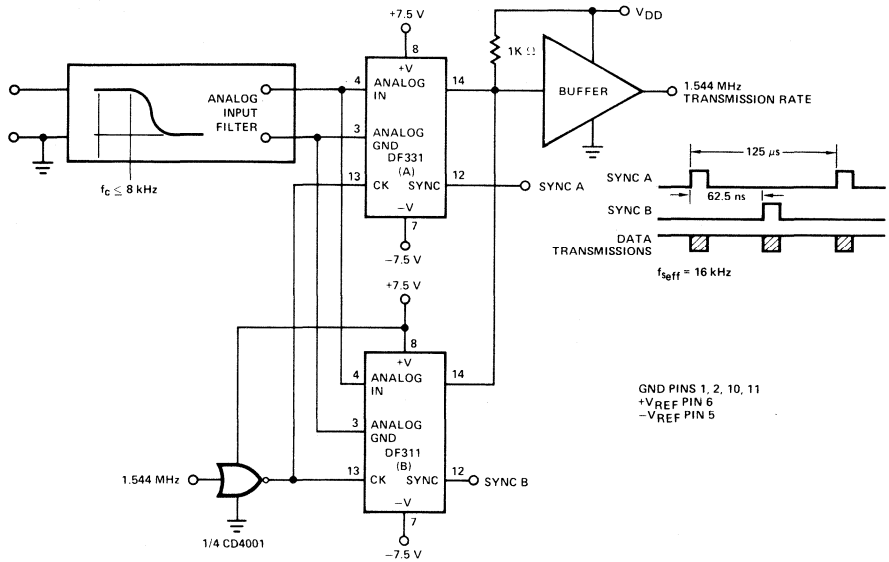
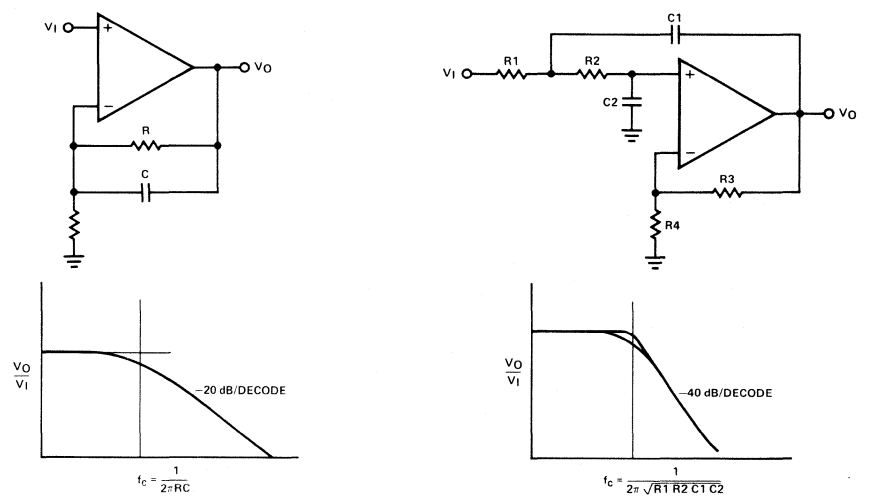


Figure 4



Single Pole Filter **Double Pole Filter**

Simple Filter Implementations
Figure 5

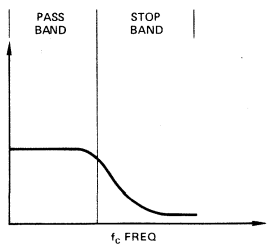
Higher Order Filters (3rd Order and Higher)

Butterworth filter is considered the maximally flat filter in the pass and stopband as shown in Figure 6. You are giving up sharp cutoff frequency when using this implementation compared to the next two approaches. This filter has all zero's at infinity.

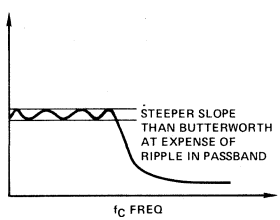
Chebychev filter trades flatness in the passband for sharp cutoff at f_c. It can be shown that the Chebychev has the steepest descent into the stopband of filters constructed with all zero's located at infinity. This filter approach is used in the evaluation filter that follows.

Elliptic filters obtain the steepest slopes into the stopband by positioning their response zeros near the passband. The zeros cause the lobes in the stopband (Figure 6). This approach does meet the stringent requirements of a D3 channel bank in the telecommunications industry. Element value tolerances are the most critical in elliptic filters. As a general rule, the more complex the filter calculations become, the tighter the required component tolerance.

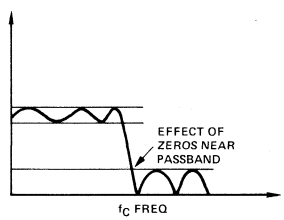
The filter approaches listed are traditional approaches that, at best, must be constructed as hybrid circuits with precise laser trimmed resistors. A monolithic integrated circuit is out of the question as a manufacturable approach using traditional resistors, capacitors and inductors due to the precision requirements and large component values.



Butterworth Maximally Flat Response



Chebychev Filter



Elliptic Filter

Comparing Butterworth, Chebychev & Elliptic Filter Responses
Figure 6

EVALUATION FILTER

In most applications outside of telecommunications the filter shown in Figure 7 will provide good performance in interfacing the CODEC to different transducers (e.g. strain gauges, audio pickups, accelerometers, etc.). The filter is a 6th order multiple feedback filter whose design is outlined in reference [1]. It is an all-pole filter (zeros all at ∞) which results in no lobes in the stopband.

The choice of this filter and components was made on the following criteria:

1. The overall feedback from all three stages reduces the sensitivity to component tolerance compared to the 2-pole per stage cascaded approach.

2. The 6th order response results in −9 dB attenuation at one-half f_S and −45 dB attenuation at f_S adequate for both the transmit and receive filter locations.

3. When this filter is used in the receive position (output of DF332) it does not compensate for the cutoff frequency attenuation introduced by sampling (sin x/x effect).

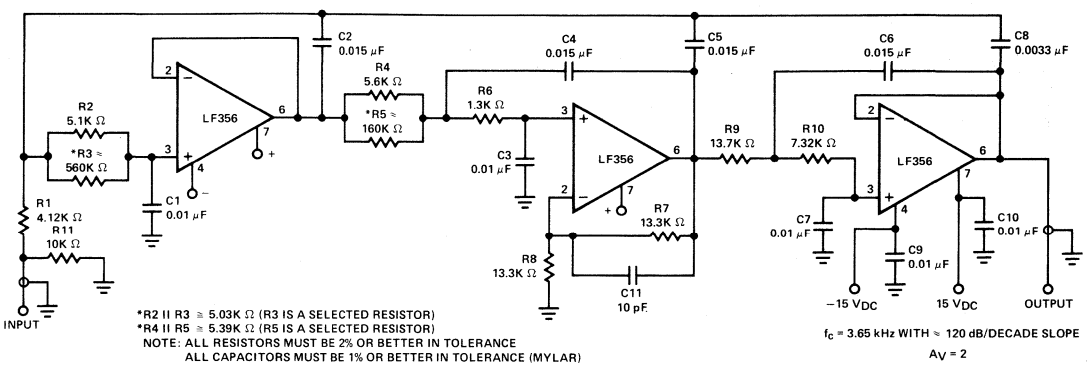
4. The choice of LF356 op amps was made for their high input impedance (minimum circuit loading), low output impedance (ability to drive capacitive loads) and wide bandwidth.

5. The effective output impedance of this filter adequately drives the input sampling current requirements of the DF331 encoder.

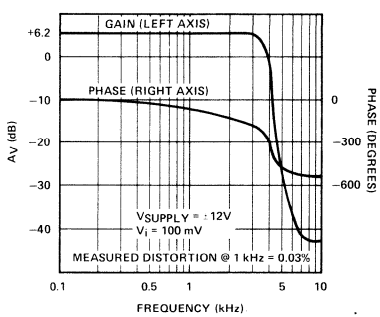
The gain and phase versus frequency response of the filter is shown in Figure 8. An HP3575A gain-phase meter was used for this measurement.

REFERENCES

1. D. Johnson, *Rapid Practical Designs of Active Filters,* Wiley 1975.
2. Technical Staff Bell Telephone Laboratories, *Transmission Systems for Communications,* fourth edition, 1971.
3. P. Geffe, *Simplified Modern Filter Design,* Hayden, New York, 1964.
4. The D3 Channel Bank Compatibility Specification–Issue 3, Oct. 1977. Technical Advisory No. 32 (This information is assembled by AT&T for distribution to non-Bell companies. It represents current plans and is subject to subsequent change.)



Multiple Feedback Low Pass Filter of the 6th Order
Figure 7



Performance of 6th Order
Multiple Feedback Low Pass Filter
Figure 8

Siliconix

Designing with codecs: know your A's and μ's

Nonlinear coders/decoders, or codecs, require your familiarity with framing, synchronization and signaling. Here's a brief intro.

Thomas J Mroz, Siliconix Inc

When designing telecommunications circuits using nonlinear A/D/A conversion, you'll choose from parts that conform to either the Bell Telephone-specified μ-255 Law or the CCITT (International Telegraph and Telephone Consultative Committee)-specified A Law, if you want to guarantee compatibility with other systems. While the first sees wide usage in North America, most of the world uses the second. These conventions govern the same basic operation—analog signal expansion and compression—but differ in their data formats. The differences become apparent upon examination of channel-bank concepts.

Channel banks translate voices into bits

Today's phone systems employ mazes of switches and filters for both analog and digital signals. One small part of these complex networks, the channel bank, transforms analog voice signals at a local exchange into easily transmitted digital signals. It's then easy to compress, transmit and repeat these digital signals in cable and microwave transmissions.

Circuits termed coders sample the analog voice signals generated by user phones, convert them to digital bytes and shift them serially out of the channel bank. On the receiving end, decoders accept these bytes and recreate the analog voice signals initially generated by the phone user. The term *codec* applies to a complete coder/decoder (A/D/A) set.

Channel banks, located in telephone-company central offices, use codecs to handle many phones, encoding analog voice signals into serial data streams for transmission to various receiving banks. One bank can also decode incoming calls and redistribute analog voice signals to user phones **(Fig 1)**. Both codecs and channel banks follow specifications in the μ-255 Law or the A Law that not only govern transfer characteristics, but also define formats for framing, synchronization and signaling.

Pulse-code modulation (PCM), the technique channel banks employ to transmit and receive information, allows them to sample analog inputs

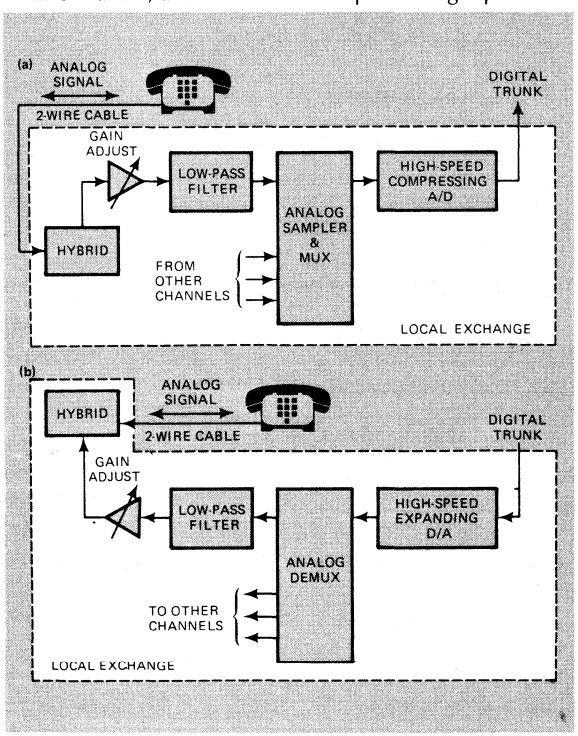


Fig 1—Most existing phone systems employing pulse-code modulation (PCM) use just one high-performance data converter in the transmitter **(a)** or receiver **(b)**. Multiplexers make these converters available to all the channels the exchange handles. In these diagrams, a hybrid is a device that converts 2-wire phone signals to 4-wire signals, thus eliminating crosstalk between incoming and outgoing data.

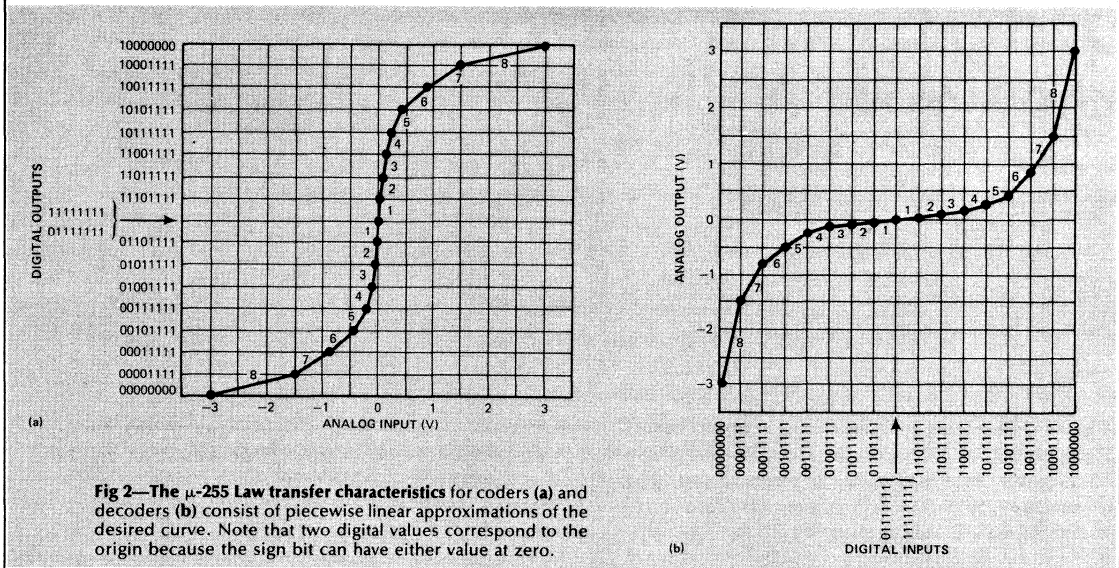


Fig 2—The μ-255 Law transfer characteristics for coders **(a)** and decoders **(b)** consist of piecewise linear approximations of the desired curve. Note that two digital values correspond to the origin because the sign bit can have either value at zero.

at a fixed rate and then perform an A/D conversion that quantizes the sample into an 8-bit sign-plus-magnitude word.

Coder and decoder nonlinear transfer characteristics **(Figs 2, 3)** maintain relatively constant signal-to-distortion (S/D) levels over a wide range of analog input levels. Because the channel bank compresses high input levels and expands low levels, a person speaking softly into a phone is nearly as intelligible as someone speaking loudly. Thus codecs are termed companding A/D/A converter sets.

How do the μ Law and A Law differ?

The μ-255 Law and A Law differ fundamentally in the transfer characteristics associated with their

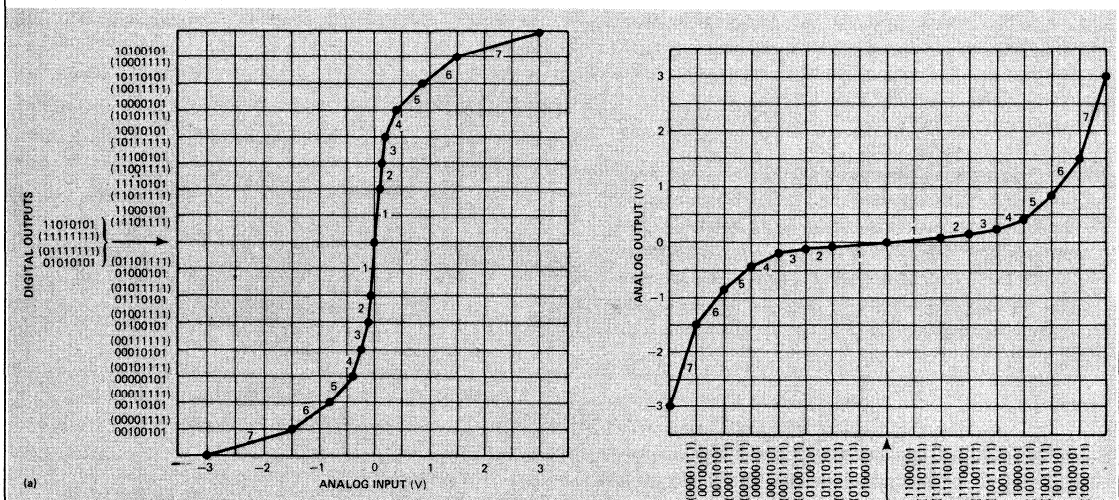


Fig 3—The A Law transfer characteristics for coders **(a)** and decoders **(b)** reduce the number of chords required in μ-255 Law curves by making chords near the origin colinear. Note that values listed in parentheses are the corresponding μ-255 Law values.

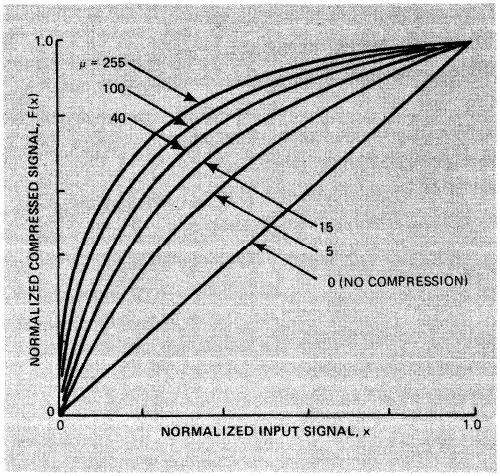


Fig 4—Logarithmic compression characteristics for the μ-255 Law equation show that μ=0 corresponds to linear operation; large μ values provide increased compression.

A/D and D/A conversions. The equation

$$F(x) = \text{Sgn}\ (x)\ \frac{\ln\ (1 + \mu\ |x|)}{\ln\ (1 + \mu)}$$

defines the μ-255 Law (where μ=255). A coder's A/D converter approximates this equation, while a decoder approximates the equation's inverse.

Two important equations apply to the A Law:

$$F(x) = \text{Sgn}\ (x)\ \frac{1 + \log_{10} A\ |x|}{1 + \log_{10} A} \text{ for } \frac{1}{A} \leq |x| \leq 1$$

$$F(x) = \text{Sgn}\ (x)\ \frac{A\ |x|}{1 + \log_{10} A} \text{ for } 0 \leq |x| \leq \frac{1}{A}$$

where A=87.6.

Examining the μ-255 Law equation, you can see that μ=0 represents a linear conversion; increasing μ increases the converter's nonlinearity or compressing characteristics **(Fig 4). Fig 5** illustrates the ability of nonlinear converters to maintain fixed S/D ratios over wide dynamic ranges.

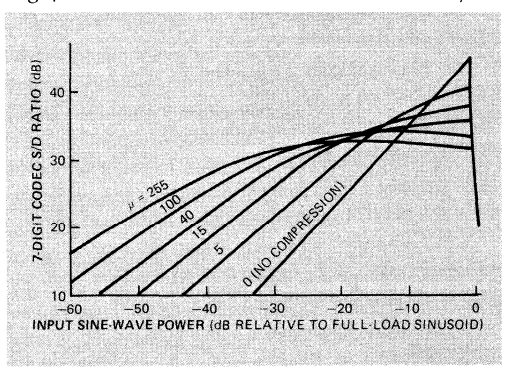


Fig 5—Signal-to-distortion performance of logarithmic compandors remains fairly linear for low-power signals independent of the value of μ.

Actual devices such as codecs approximate these equations in piecewise linear fashion. The 8-bit digital code has a sign bit, three bits for chord selection and four bits for step selection within the chord. Thus the μ-255 Law uses a 15-segment approximation (16 segments if you break the line through the origin in half). The A Law, on the other hand, combines the two μ-255 Law chords centered about the origin; making them colinear reduces the number of chords needed. Thus the A Law employs a 13-segment curve.

These differences in chord count reflect conversion conventions in the first step about the origin. **(Fig 6).** The μ-255 Law indicates that an analog input voltage relating to a digital output of zero should be half as large as the analog input span related to the next digital step—called a midstep condition with a silent interval. The A Law requires no silent interval and employs a mid-riser condition where the origin represents an indeterminate (bistate) digital output. But once past these first several chord segments, the two laws are identical.

Channel banks can use different circuit configurations to accomplish the same task. In the past, one A/D/A set encoded many voice channels, requiring analog multiplexing of these channels, along with a high-speed codec. Multiplexing after the A/D conversion could greatly reduce channel crosstalk, and per-channel codecs such as the Siliconix DF331/332 make this type of system easy to construct. Although implemented with CMOS, DF331/332's have NMOS open-drain digital outputs. Thus, while the per-channel approach eliminates the need for an analog MUX, open-drain outputs tied together eliminate the need for a digital MUX **(Fig 7).** These two factors, eliminating crosstalk problems and analog multiplexers, have stimulated much interest in per-channel codecs within the telecommunications industry.

Frame formats structure multiplexed data

Multiplexing many analog voice channels after conversion into one serial data stream requires a method for synchronizing transmitters and receivers, so that channel banks can transmit digital information in a frame format. Under the μ-255 Law, a frame consists of 24 channels or 24 bytes of digital information **(Fig 8a),** with one data bit dedicated as a framing bit—a definition resulting in a total of 193 bits/frame. The μ-255 Law specifies that these data bits be transmitted at 1.544M bps.

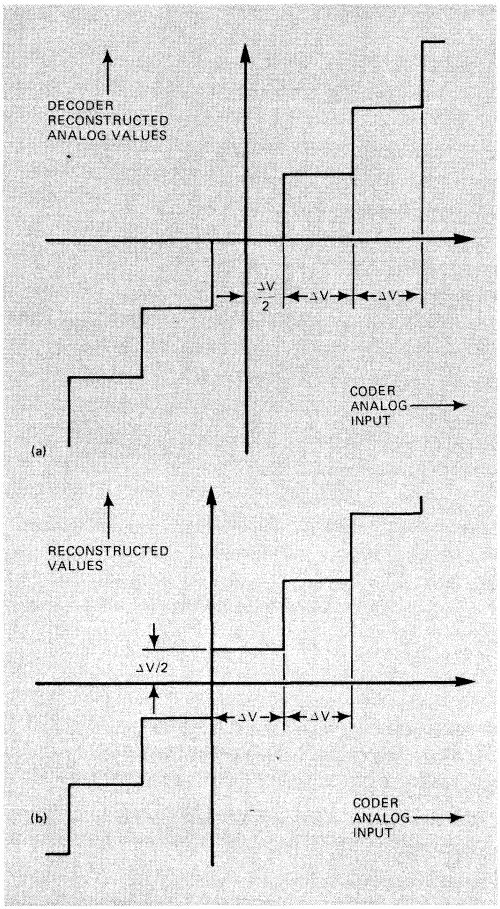


Fig 6—If you examine the first steps of μ-255 Law **(a)** and A Law **(b)** coder transfer characteristics you'll see an important difference: the μ-255 Law experiences a midstep condition with a silent interval while the A Law sees a mid-riser condition. Output coding differences reflect this discrepancy.

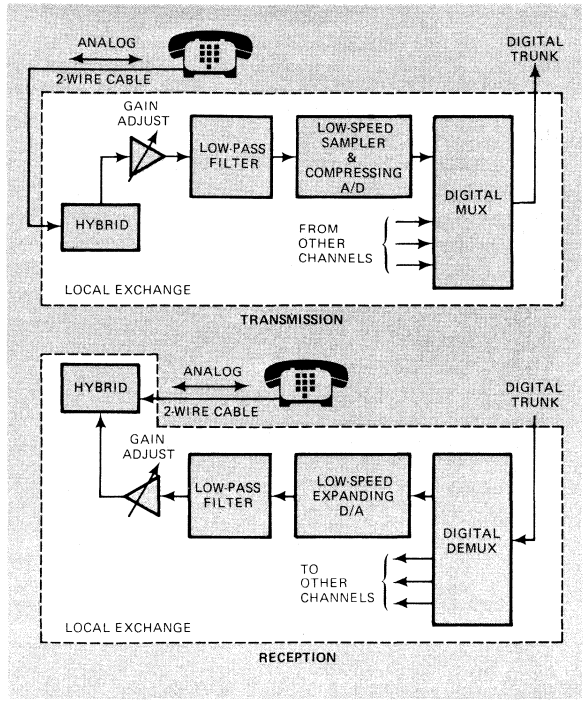


Fig 7—Per-channel coding/decoding of voice signals in new-design channel banks uses inexpensive IC codecs for each channel and multiplexes digital signals for cable transmission. This technique, simpler and cheaper to implement than analog multiplexing, also eliminates analog sampling crosstalk.

The A Law also employs a framing concept, but with a data-transmission rate of 2.048M bps, thus allowing enough time to transmit 32 8-bit words for each frame. Another difference: The A Law doesn't generate a framing bit as in μ-255 Law channel-bank systems; rather, it dedicates a complete channel time slot to framing **(Fig 8b).**

Although a frame equals the time required to transmit one byte of data for each channel, still needed is a way to identify individual channels in the transmitted data stream. Previous designs synchronized the analog multiplexers in front of the A/D in the transmitter to those on the receiving end. New designs incorporating the DF331/332 codec set in a per-channel configuration use sync pulses. These pulses, ANDed with a clock, dump or load output or input shift registers that reside on the coder and decoder. Because channel-bank transmission-line lengths vary, received data looks asynchronous. Therefore you must derive clock and sync signals for the receiving channel bank from the incoming data.

New μ-255 Law codec designs must also accommodate signaling capability. Signaling information lets the transmitting and receiving banks communicate information such as alarms, off hook and on hook, and it checks to ensure that the banks operate in sync.

Under the μ-255 Law, every sixth frame becomes a signaling frame; thus the eighth bit of every channel carries signaling information presented at that channel. In other words, the bank performs 7-bit A/D/A conversions during a signaling frame, reserving the eighth bit-time slot for the signaling bit. By contrast, the A Law uses reserved-channel signaling, which dedicates to signaling one entire channel out of the total 32 in each frame. Thus, signaling frames don't exist as in the μ-255 Law because signaling occurs in every frame.

When testing and evaluating channel-bank performance, realize that it's only fair to simulate human limitations. You can accomplish this objective by inserting a C-message filter **(Fig 9)** in front of equipment used to test noise and distortion in the complete A/D/A path. Such filters simply simulate the human ear's frequency response to noise; weighting during measurements guarantees that measured distortion levels and noise relate directly to human ability to understand phone conversations.

The three most important codec specs

All new designs aimed at upgrading systems share a common goal: to meet or exceed existing specifications. Codecs face pressure on three important specifications: S/D ratio, idle channel noise and gain tracking. These specs will make or break new codec designs.

Because of codec nonlinear conversion techniques, the specifications generally appear as functions of input power ranges. Signal-to-distortion figures simply give the ratio of the signal power to the distortion power created by quantization errors and internal noise **(Fig 10a).** Thus, specs for S/D ratio cover the following input power ranges:

P_{in} = 0 to −30 dBm0
= −30 to −40 dBm0
= −40 to −45 dBm0.

As a reference level, 0 dBm represents a 1 mW test tone, and the term dBm0 refers to relative power at the input. As an example, consider a transmission line with 3 dB loss to the end point. You would refer to −50 dBm of noise at the endpoint as −47 dBm0, and the line endpoint would be a −3 dBr point (relative to input).

Idle channel noise measures the noise power seen at the receiving end of the system with 0V on a transmitting channel's input. The last spec of interest, gain tracking **(Fig 10b)**, relates system gain to input power level.

These specifications define a system spec and imply that any new device intended to replace portions of existing systems must exceed these ratings by a suitable margin. For S/D ratio, the suitable term translates into several decibels; idle channel noise should be as low as possible, but certainly at least 5 dB better than system specs.

Codecs see a promising future

With the introduction of new codec IC's, a new world of application possibilities arises. In discrete form, these system components formerly required large areas and substantial investments in design time, making the cost of incorporating them into systems outside of telecommunications

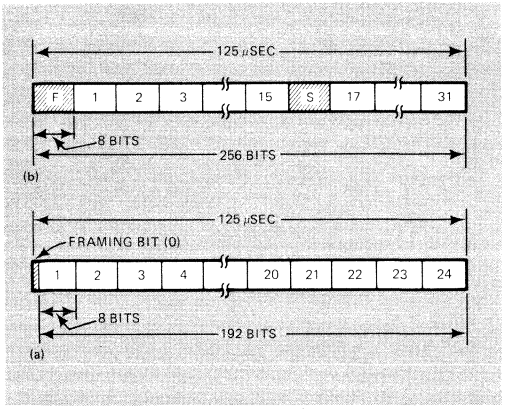


Fig 8—Frame formats place channel data in preassigned time slots. The μ-255 Law uses one framing bit every 24 bytes **(a)** with each byte corresponding to data from one channel. The A Law format **(b)** dictates complete channels for framing and signaling data.

prohibitive. Now, codecs of the same quality are available at costs comparable to those of other mass-produced integrated A/D converters. Applications such as audio delay lines (digital form), portable communications using PCM, remote data acquisition and talking computers are becoming realizable and less expensive to develop and produce.

Because parts such as the present codec IC's arose primarily to serve the communications industry, their quality and function in other applications are guaranteed; the telecommunications industry sets very high standards of accuracy and reliability. The elimination of adjacent-channel crosstalk through the per-channel codec approach leads to major quality improvements in voice transmission over PCM communication links.

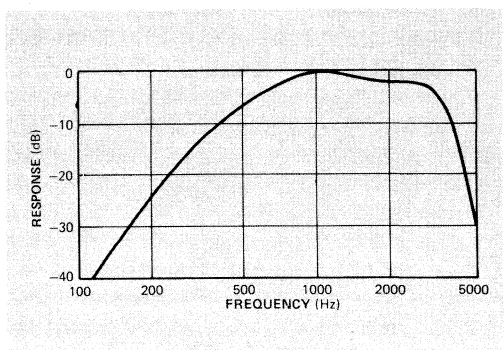


Fig 9—C-message frequency weighting simulates the response of a Model 500 telephone and voice characteristics of average phone subscribers when relating noise and distortion effects to voice-signal intelligibility.

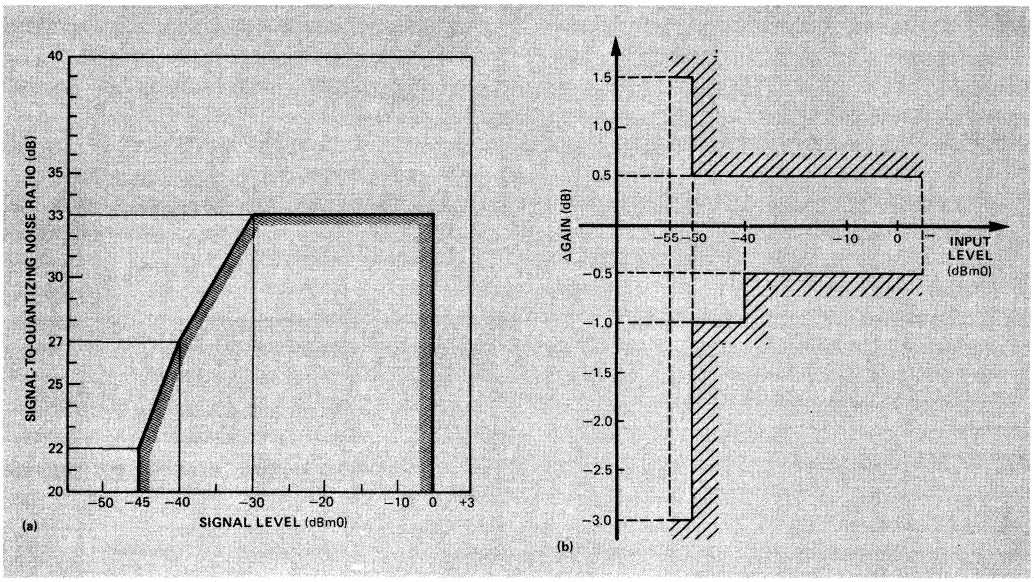


Fig 10—Codec IC's must meet performance standards in several important areas. Minimum specs for S/D ratio **(a)** and gain tracking **(b)** apply to both μ-255 Law and A Law systems. Note that ΔG represents system gain measured from the coder's input to the decoder's output and also gives an analog ratio.

Additionally, codec nonlinearity aspects offer some interesting alternatives to linear converters. The 8-bit data format covers a 72 dB dynamic range (equivalent to 12 bits) and lets you easily interface inputs from wide-dynamic-range natural phenomena, such as wind speeds or earthquakes, to popular 8-bit μC's. In voice-synthesis applications, codecs give computers more realistic voices. Additional codec applications will result as design information increases. □

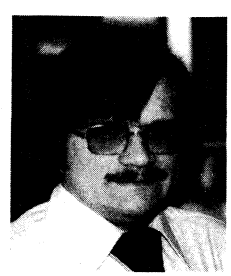
References

1. Bell Telephone Laboratories, Transmission Systems for Communications, Western Electric Co Inc, 1970, pgs 566-583.

2. International Telephone and Telegraph Corp, Reference Data for Radio Engineers, Howard W Sams & Co Inc, 1968, pgs 2-1,2.

3. American Telephone and Telegraph, Data Communications Using the Switched Telecommunications Network, 1970.

Author's biography



Tom Mroz develops telecommunications, timing and interface circuits as a design engineer for Siliconix, Santa Clara, CA. After earning his BSEE at Purdue Univ, he worked for Motorola Semiconductor Products Div and then joined Siliconix in March 1976 as an applications engineer. Among his hobbies Tom lists photography, boating, woodworking and listening to classical music.

Reprinted from **EDN** May 5, 1978

Siliconix

CODEC HAS ON-CHIP SIGNALING FOR PHONE APPLICATIONS

Walt Heinzer
Steve Bolger

Putting coding and decoding functions on two separate chips also cuts out crosstalk and increases design flexibility

☐ For the would-be codec user, the separation of the encoding and decoding functions onto two chips has many advantages. Such a configuration is low-cost, guarantees high isolation between the transmitting and receiving operations, and allows him considerable freedom of design.

Each chip of such a pair is smaller than a one-chip codec, so that reliability and yields are higher and cost lower. Each fits in a 14-pin package, so that board layout is compact. Being isolated from one another, coding and decoding can be carried out asynchronously, as need be, and crosstalk between the two directions of voice travel is completely eliminated.

Moreover, using minimal support circuitry, the designer can lay out his system in a variety of ways—on single-channel codec cards, for example, or on multiple-channel receive-only and transmit-only cards that minimize the amount of digital busing that will be needed on motherboards.

Another plus

All these advantages and more accrue to Siliconix' complementary-MOS encoder and decoder chips, the DF331/DF332, the first codec chip set to be introduced. For in addition, these chips include signaling functions in both their μ-law and A-law versions. This feature makes them particularly effective and easy to use in channel bank or central office applications.

One member of the pair provides the complete encoder analog-to-digital conversion function, the other the complete digital-to-analog conversion function (Fig. 1). Each of the chips has the same basic requirements for power supplies, voltage references, clock signals, and synchronization pulses. All digital data is time-division-multiplexed into a single serial bit stream.

The C-MOS technology with which the pair is built is well able to meet governing AT&T channel bank specifications. These specifications require a codec to have a precise dynamic signal response over a range of audio frequencies. This response is measured in terms of gain tracking, signal-to-noise distortion ratio, and channel noise and must also have certain quantization levels and timing and data formats. When the need for low power consumption was added to these considerations, C-MOS appeared the best integrated-circuit technology to use.

The ± 7.5-volt ($\pm 10\%$) power supplies required for each chip keep power dissipation low, to an average of only 40 to 45 milliwatts per device. The supply voltages are easily obtained from a discrete regulator supply circuit or from standard three-terminal regulator chips.

These reasonable power dissipation levels do not impair the codec's analog system performance. Both the Bell System's D-3 specification and the CCITT recommendations are readily met. What is more, any encoder is guaranteed to function properly with any decoder since the analog performance is specified on a per-part basis. For example, the signal-to-noise distortion ratio exceeds the requirements by at least 6 decibels over all input ranges (4 dB for signaling every sixth frame, as required by the μ law). Gain tracking is typically ± 0.15 dB per part for input levels from $+3$ to -45 dBm and $+0.25$ dB per part for -45- to -55-dBm inputs.

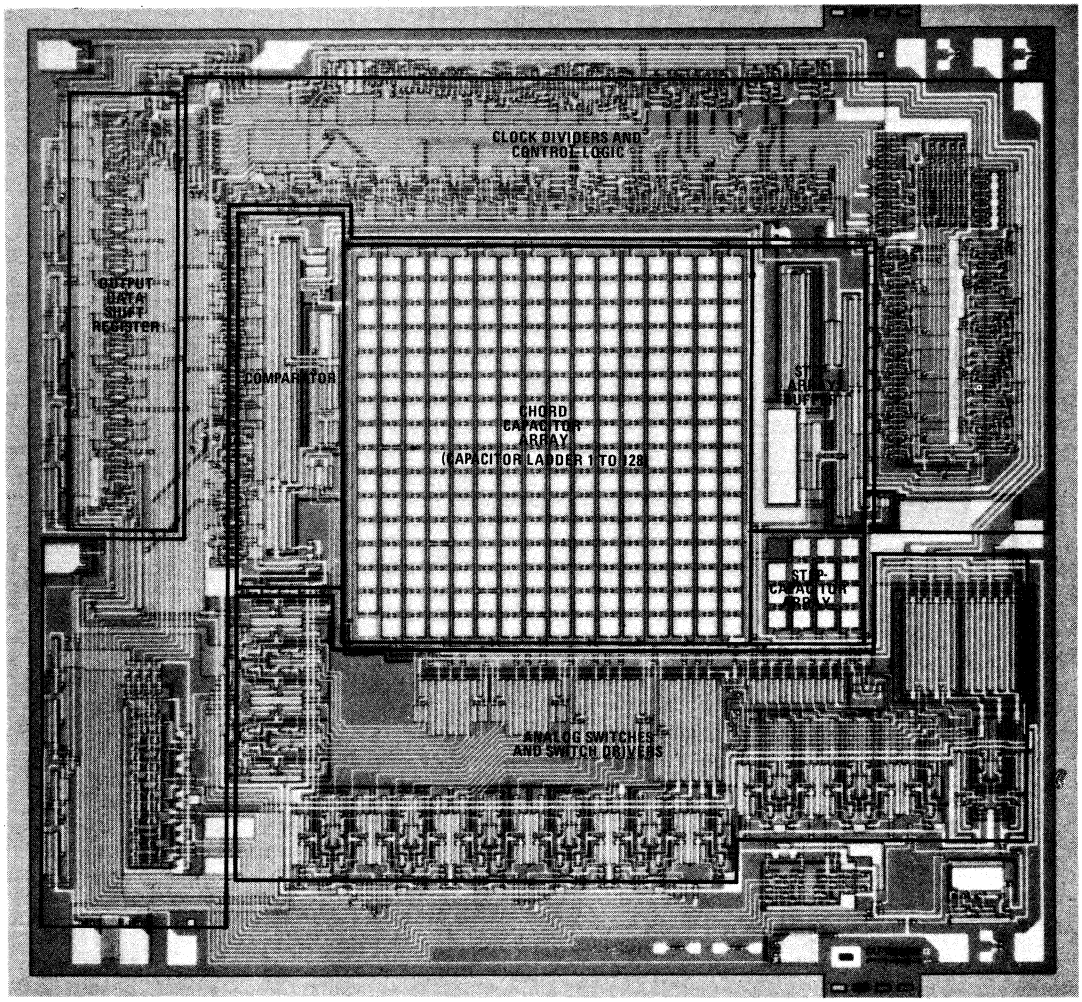
A standby condition reduces power dissipation still further, typically to 11 mW for the codec pair. The two devices are switched into the standby condition by using C-MOS-logic–compatible switches to open the analog ground line, thus turning off the current sources to the analog circuitry that uses most of the codec power. In this standby mode, synchronization pulses to the decoder should be stopped. Otherwise its output sample-and-hold circuitry will slew to either the positive or the negative codec voltage reference signal as it tries to decode.

Keeping on track

The reference voltages are important to the performance of a codec's analog system. They serve both the a-d and d-a conversions and are crucial to achieving proper gain levels throughout the system. For the Siliconix design, external voltage references were chosen for their cost-effectiveness, accuracy over the long term, and independence of the codec chips. They minimize the effect of codec manufacturing tolerances on system gain and temperature stability since the responsibility for gain and long-term drift is shifted to an external and therefore easily controlled, maintained, and designed source.

The approach yields an absolute gain accuracy of

Reprinted from ELECTRONICS, June 7, 1979



1. One of a pair. The DF331 encoder shown combines with the DF332 decoder to provide a codec complementary-MOS chip pair. Asynchronous operation is simplified with this approach and crosstalk between transmitted and received voice signals is virtually eliminated.

typically ±0.2 dB from device to device, making the codecs interchangeable without additional channel gain adjustment. The ±3.0-V external voltage reference also sets the maximum allowable input signal level. Given a system dynamic range of 72 dB, this also means the minimum signal-to-noise ratio will be relatively large.

To obtain the best system signal-to-noise ratios and to minimize gain error, the positive and negative references must track within 1% of each other. They are also used by the a-d and d-a converters to determine the voltage step sizes to be employed in the conversion—a critical process. These codecs perform the conversions with a successive-approximation technique using weighted capacitive arrays (see "Capacitors make stable converters," p.136). As the reference levels are the over-range levels of the converter, the maximum digital signals correspond to ±3.0 V.

Both encoder and decoder use a system clock synchronization pulse for logic inputs. The input logic levels are quasi-TTL-compatible (logic low of at most 0.6 V, logic high of at least 3.4 V) to allow use with TTL as well as C-MOS logic circuits. For μ-law devices, the transmission data clock rate is 1.544 MHz with a range of 1.34 to 3.0 MHz. For A-Law devices, the rate is 2.048 MHz with a range of 1.8 to 3.0 MHz.

Both μ- and A-law devices use an 8-kilohertz sample rate. Thus, the synchronization pulses have a period of 125 microseconds with a pulse width of eight clock pulses. During the sync time, the encoder shifts its digital output out of its shift register at the positive clock edges. Open-drain, n-channel MOS transistors produce this digital output by being pulled down to digital ground for logic low signals and being pulled up by a pull-up resistor for logic high, which is 5 V for TTL and 4 to 12 V

Capacitors make stable converters

The decoder uses a weighted capacitive ladder to convert analog into digital signals. Integrated-circuit capacitors, unlike their resistor counterparts, dissipate no power within themselves and the capacitance ratios can be held within closer tolerances for given layout rules. So they are ideal ratio-ing devices with which to build stable and accurate converters that must operate over the normal telecommunications temperature range.

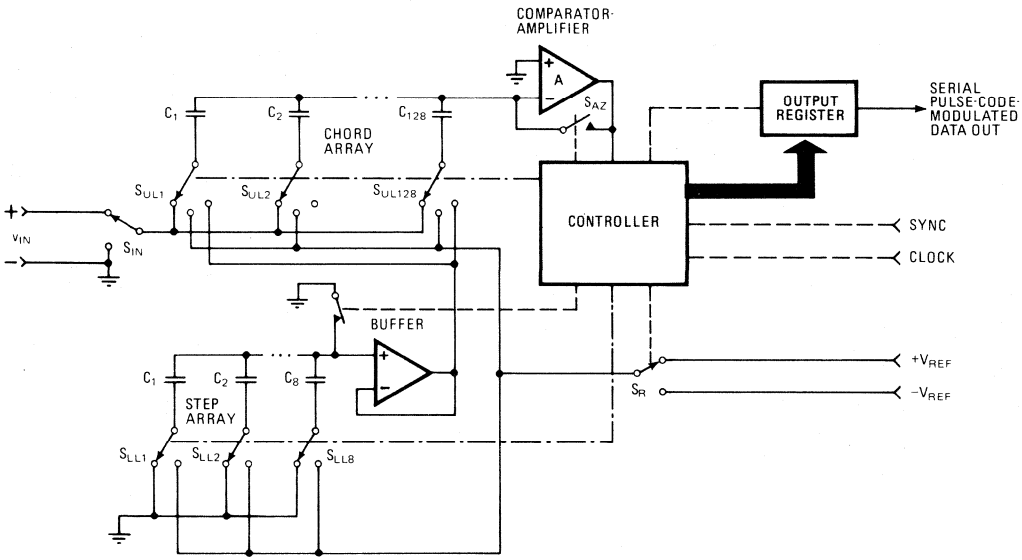
The a-d conversion process (see figure) requires a specific sequence of steps. First the analog sample is acquired. Next the sign, the chord, and the step within the chord are determined [*Electronics*, Sept. 14, 1978, p. 108]. Finally, an output shift register is loaded, the circuit is reset and returned to the sample mode, and an output is presented in the form of serial digital data.

To start the process, the receipt of the synchronization pulse initiates voltage sampling through switch S_{IN}. This voltage is stored on the bottom plate of the capacitor array. During acquisition, switch S_{AZ} is closed, placing the comparator V_{OFFSET} on the top plate of the capacitor array. Comparator A acts as a unity-gain buffer. At the end of the sampling time, the capacitor array, acting as a sample-and-hold, is charged to $-V_{IN}+V_{OFFSET}{}^{(A)}$.

After acquisition, the top plate is floated (S_{AZ} opened) and the bottom plate is shorted to ground (S_{IN}). The output of the comparator represents the polarity of the signal with the offset nulled out. Since the polarity of the signal is now known and present at the output of the comparator, the controller switches S_R to the appropriate reference.

The upper ladder switches (S_{UL}) are then connected in a successive-approximation sequence to determine the proper chord. Charge redistribution takes place on the capacitive ladder, continuously updating the voltage presented to comparator A.

Finally, the lower ladder is switched in a successive-approximation sequence to determine the appropriate step within the previously determined chord. Only at this point does the digital result of the conversion load the output register.



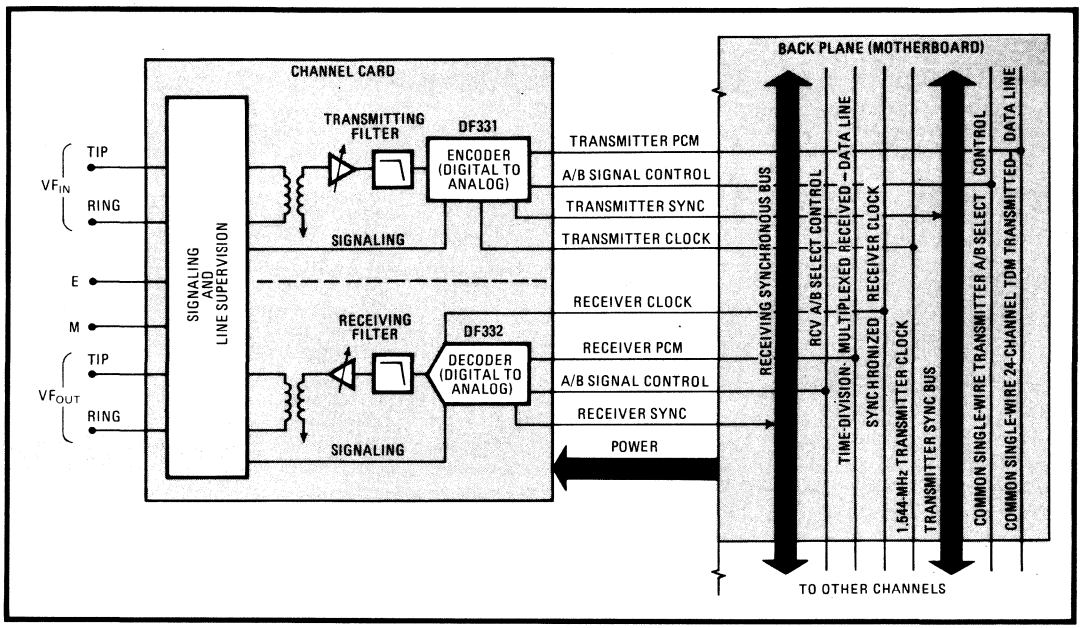
for C-MOS. If several encoders are being used, they are wire-ORed together so as to time-division-multiplex their outputs onto a single pulse-code-modulated data line.

The rates for encoding and decoding differ since the decoding d-a conversion is a faster operation. Decoding takes less than 15 μs and resetting the chip results in a total conversion time of 25 μs. Encoding requires a total of 108 μs to do the sampling, successive approximation, and resetting operations.

Channel bank signaling

The signaling functions included on the codecs ensure their simplicity and flexibility of use in channel bank applications. For the American μ-law family, the signaling occurs every sixth frame in the data stream. Each frame consists of 193 bits: 24 8-bit data words, each time-multiplexed into its own time slot, plus 1 framing (S) bit. During each signaling frame, the 8-bit conversion yields only 7 data bits, the 8th being used as a signal bit for transmitting and receiving supervision and signaling information. The encoder contains logic inputs for the A signal input, B signal input and A/B select. The A/B select input is an edge-sensitive input that tells the chip to encode a signaling input into the 8th bit position in the pulse-code(d)-modulated (PCM) data stream.

At the decoder, the A/B select logic input tells the chip to take the 8th bit and transfer the data to the A or B signal output pin. During signaling, the decoder's digital-to-analog converter still needs 8 bits, but since the data word has transferred only the most significant 7



2. Channel card. The encoder chip that converts analog into digital signals and the decoder chip that does the reverse are typically mounted on a separate channel card for an individual telephone. All control signals and power, however, come from the motherboard.

bits, an average value of a logic 0 and a logic 1—logic ½—is assigned to the 8th and least significant bit. The assignment of a ½ bit in the LSB position enhances a system's signal-to-noise distortion ratio at low signal levels by making a smooth transition through the origin of the analog-to-digital transfer characteristic.

Thus, these μ-law codecs readily produce the signaling logic required for channel bank operations. Adding to design flexibility, all channels can have the A/B select transition occur at the beginning of the signal frame, eliminating the need for separate A/B select lines for each channel.

In the A-law format, signaling is done on the 16th time slot of every frame in the data stream. The A-Law encoder incorporates the necessary gated signal logic—a NAND gate with two inputs, one the signal and the other a sync NANDed to the signal-out open-drain n-MOS transistor. This setup allows each encoder to gate any signal information with its sync pulse and tie all of the channel signal-out information to a common digital signal output line.

External capacitors for sampling and holding or automatic zeroing are unnecessary. The encoder samples the input signal, while the internal capacitor array performs the necessary sample-and-hold function. The capacitor array also stores the necessary charge for auto zeroing.

A phone system

The benefits of keeping a coder and decoder separate are also evident in a phone system (Fig. 2). In this application a typical per-channel codec has a four-wire interface located between toll centers. Voice paths are completely divided, even on the channel card.

The PCM transmitter data and clock lines require separation from the PCM receiver data and clock lines since the timing controls are several tens of miles apart. The problem here is that the phases of the two clocks and even the fundamental frequency will be different. These differences make it difficult to design a single-chip encoder/decoder such that interactions like beat frequencies will not occur between the two data paths. But a two-chip model of its nature guarantees the necessary isolation.

Easy interface

The Siliconix codec also eliminates the external logic often necessary to interface between the four-wire signaling and the μ-law signaling formats. Its common A/B select control line for all channels in the channel bank simplifies the loading and unloading of signaling data into every sixth frame. The loading and unloading of 24-channel PCM data onto the signal wire data bus is controlled by the time-slot generator. The PCM binary data signal is converted into a bipolar signal in the digital line driver interface. The bipolar signal is then transmitted over the 1.544-MHz twisted pair.

At the receiver, the serial bipolar data is reconstructed as a binary PCM data stream and a new clock rate derived from it. This clock rate serves as the basic timing device for the controller and all receiving circuitry, since delay variations in the carrier prohibit use of a totally synchronous system clock.

Receiver resynchronization to the incoming bit stream is accomplished by the framing (S) bit, which is present at the beginning of each 193-bit frame and handles both frame and signal synchronization. □

Appendices

CODEC/Filter Level and Noise Measurements

REFERENCE LEVELS

The overload level (full scale) for the CODEC is 3 V peak. All performance measurements are made with respect to this 3 V peak full scale level. For the D_3 channel bank, the 0 dBmO test tone level is 3 dB below the overload level. Since 3 dB below 3 V peak is

3 V (0.707) = 2.12 V peak
or 2.12 (0.707) = 1.5 Vrms,

1.5 Vrms corresponds to 0 dBmO for the CODEC. Most instruments are calibrated in 600 Ω but read voltage. Therefore, a 0 dBm (1 mW) meter reading will be given for an input voltage of

$$E = \sqrt{PR} = \sqrt{10^{-3}\,(0.6)\,10^{3}} = \sqrt{0.6} = 0.775 \text{ Vrms}$$

When reading 1.5 Vrms, the meter will indicate

$$20 \log \frac{1.5}{0.775} = 20 \log (1.935) = 20\,(0.287) = +5.74 \text{ dBm}$$

Therefore, to convert to dBmO, 5.74 dB must be subtracted from the meter reading. Alternately, a 5.74 dB attenuator pad could be inserted in front of the meter to make it read directly in dBmO.

When using a generator with built-in meter which measures its generator output (such as the HP3551A), one cannot insert a pad in front of the meter when it is in the send level measuring mode. To get the correct output level one must either set the indicated generator output level 5.74 dB higher than the desired dBmO level or insert an amplifier which has 5.74 dB voltage gain at the generator output. This will make the meter read directly in dBmO.

Since harmonic distortion, gain tracking and signal to quantizing noise ratio are a function of signal level, it is important that the above correction factors are taken into account when signals are applied and measurements are taken. Also, noise measurements in dBrnc must be converted to dBrncO by subtracting 5.74 dB from the dBrnc reading (unless the pad has been inserted to make the meter read directly in dBrncO). Notice also that if there are any other voltage gains or losses in the signal path, their effect on readings and signal levels into the CODEC must be taken into account.

Siliconix

Publications Index

Application Notes

Document Number	Title
AN70-1	FET Cascode Circuits Reduce Feedback Capacitance
* AN70-2	FETs for Video Amplifiers
AN71-1	A High Resolution CMRR Test Method
* AN72-1	FETs in Balanced Mixers
* AN72-2	FETs as Analog Switches
* AN73-1	FETs as Voltage-Controlled Resistors
AN73-2	IC Multiplexer Increases Analog Switching Speeds
AN73-3	Switching High-Frequency Signals With FET Integrated Circuits
AN73-4	Junction FETs in Active Double-Balanced Mixers
AN73-5	Driver Circuits for the JFET Analog Switch
* AN73-6	Function/Application of the L144 Programmable Micro-Power Triple Op Amp
* AN73-7	An Introduction to FETs
* AN74-1	Function/Application of the LD110/LD111 3½ Digit A/D Converter Set
AN74-2	Analog Switches in Sample and Hold Circuits
AN74-3	Designing Junction FET Input Op Amps
* AN74-4	Audio-Frequency Noise Characteristics of Junction FETs
* AN75-1	CMOS Analog Switches—A Powerful Design Tool
AN76-1	Measuring High Frequency S-Parameters on the Dual Gate MOSFET
* AN76-2	Function/Application Problem Solving with the DF215 Dual Set Point Timer
* AN76-3	VMOS—A Breakthrough in Power MOSFET Technology
* AN76-4	Function/Application of the LD110/LD114 3½ Digit A/D Converter Set
* AN76-5	Function/Application of the LD130 ±3 Digit Converter
* AN76-6	DG300 Series Analog Switch Applications
* AN76-7	Function/Application of the L161 Industry's First Programmable Micropower Comparator
* AN77-1	Function/Application of the LD120/LD121 4½ Digit A/D Converter Set in Measurement Systems
* AN77-2	Don't Trade off Analog Switch Specs. VMOS—A Solution to High Speed, High Current, Low Resistance Analog Switches
* AN77-3	Function/Application of the LD120/LD121 4½ Digit A/D Converter Interfaced with an 8080A Microprocessor
* AN77-4	Function/Application of the DF331/DF332 New Companding Converter Chip Set
* AN79-1	A 500 KHz Switching Inverter for 12 V Systems
* AN79-2	Stepping Motor Controller
* AN79-3	Dynamic Input Characteristics of VMOS Power Switch
* AN79-4	Driving VMOS Power FETs

Design Aids

Document Number	Title
* DA74-1	Design Aid of the LD110/LD111 3½ Digit DVM Demonstrator Board
* DA76-1	The VMOS Power FET Audio Amplifier
* DA76-2	Design Aid of the LD130 ±3 Digit DVM Demonstrator Board
DA76-3	Design Aid of the LD130 ±3 Digit Auto-Ranging DMM
* DA77-1	Design Aid to Build a Portable 0 to 99.9 °F LCD Display Thermometer using the DF412
* DA77-2	Design Aid of the LD120/LD121 4½ Digit DVM
* DA77-3	Design Aid to Build a Smoke Alarm Demonstrator with the SM110 Detector IC
* DA77-4	Design Aid to Build a Piezoelectric Smoke Alarm Demonstrator with the SM110 Detector IC
* DA77-5	Design Aid for a Versatile Darkroom Timer using the DF215
* DA78-1	Design Aid to Build a CODEC Evaluation Demonstrator with the DF331/DF332/DF334
* DA78-2	Considerations for the Filtering of Analog Signals in DF331/DF332/DF334 CODEC Converter Applications
DA78-4	Design Aid to Build a Smoke Detector with the SM110 IC

Design Ideas

* DI71-1	The FET Constant Current Source
DI71-4	Wideband Mixer-Preamplifer Using FETs
DI71-5	A FET Frequency Doubler
DI71-6	Using FETs in Selective VHF Amplifiers
DI71-8	Using JFETs in Ultra-Wideband UHF Amplifiers
* DI71-9	Wideband UHF Amplifier with High Performance FETs
* DI73-2	High Performance FETs in Low-Noise VHF Oscillators

Technical Articles

TA70-1	High Frequency Junction FET Characterisation and Application
* TA70-2	FET Biasing
* TA73-1	Multiplexer Adds Efficiency To 32-Channel Telephone System
* TA73-2	Designing with Monolithic FET Switches
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* TA76-2	A New Technology: Application of VMOS Power FETs for High Frequency Communications
* TA78-1	Designing with CODECs: Know your A's and μ's
* TA78-2	Designing a VMOS 250 Watt Off-Line Inverter

* Available in bound catalog form only.

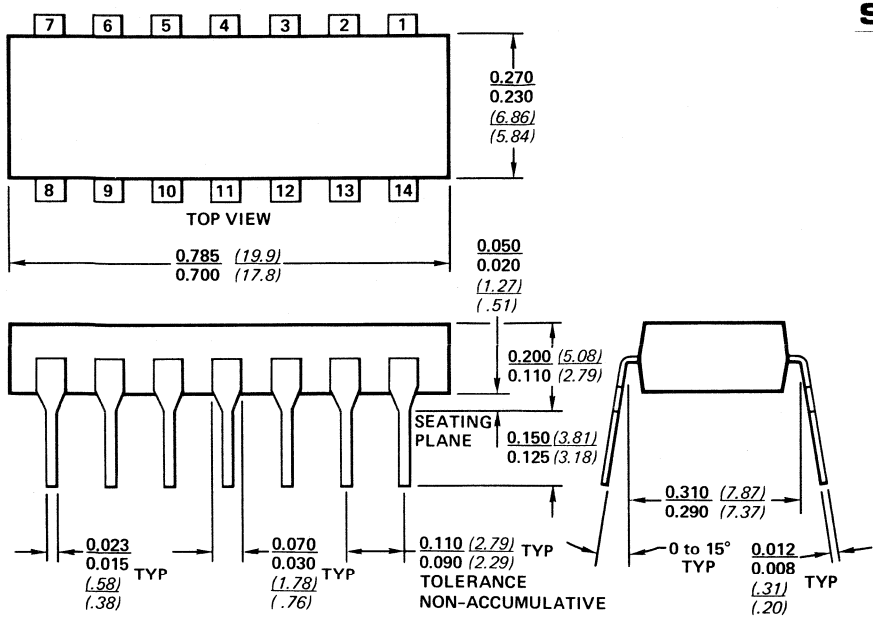
Document Number	Title
	Catalogs
_____	Analog Switch Data Book
_____	Analog Switches and Their Applications ($4.00 charge)
_____	DG300 Series Design Catalog
_____	FET Data Book
_____	LSI Design Catalog
_____	Telecommunications Data Book
_____	VMOS Power FET Design Catalog
_____	OEM Pricing/Product Information Selector Guide

Document Number	Title
	Reprints & Reports
_____	Designing a VMOS 250 Watt Off-Line Inverter. David C. Hoffman, *Power Con* 3/78
_____	Designing with Codec's: Know your A's and μ's. Thomas J. Mroz, *EDN* 5/76
_____	Log Data under μ Control. Gary Grandbois, *Electronic Design* 5/76
_____	Higher Power Ratings Extend VMOS FETs' Dominion. Arthur D. Evans, David C. Hoffman, Edwin S. Oxner, Walter Heinzer and Lee Shaeffer. *Electronics* 6/78
_____	Siliconix, Inc. Annual Report. 1979

Mechanical Data

Mechanical Data

Siliconix



PACKAGE 7
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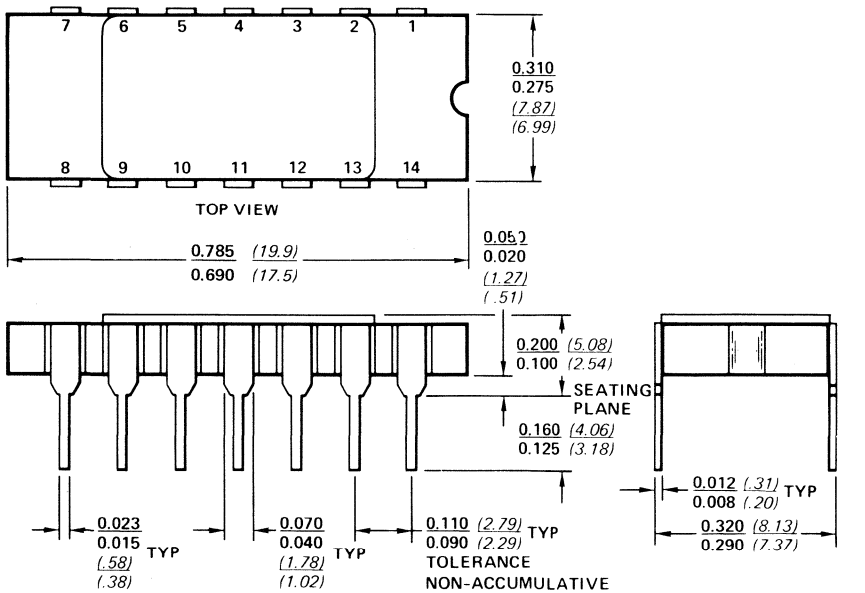

PACKAGE 11
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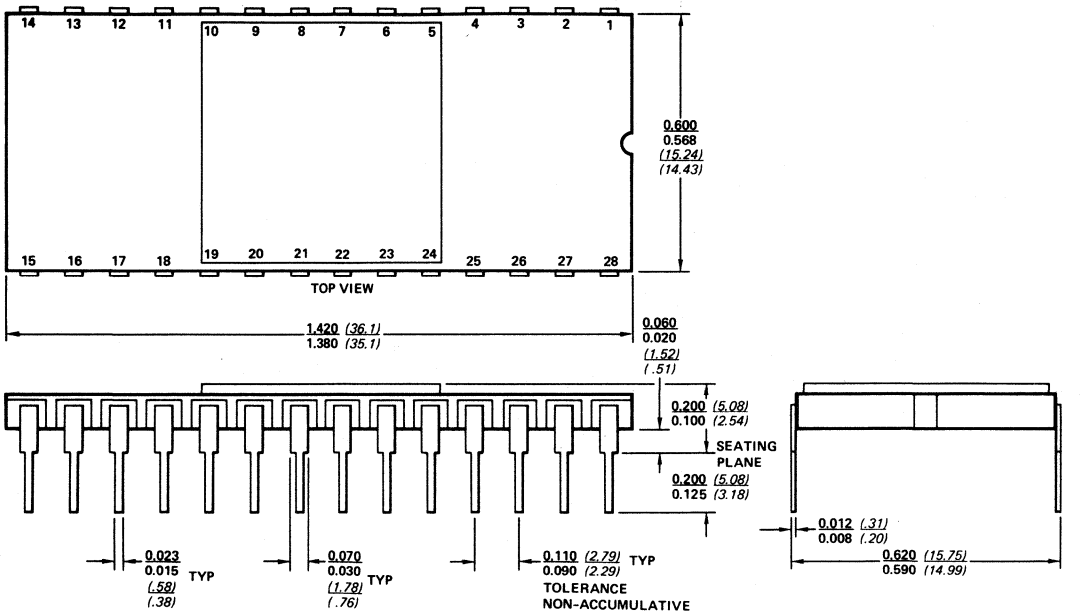
- NOTCH IN END OF PACKAGE VISIBLE FROM TOP AND/OR BOTTOM



PACKAGE 13
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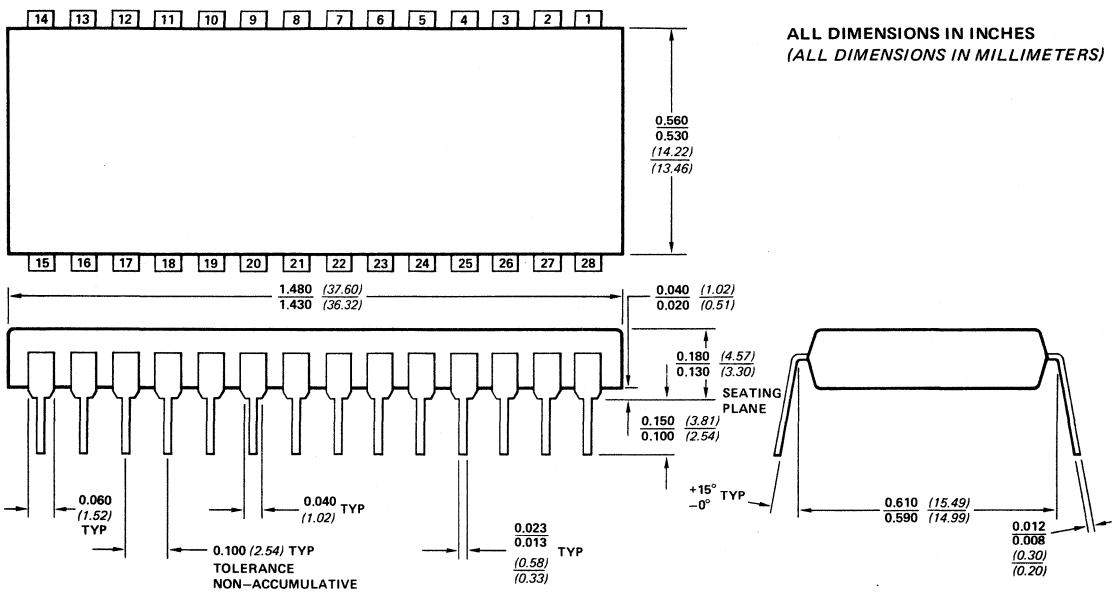

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

PACKAGE 14
28 LEAD DUAL IN-LINE PACKAGE (J)
(PLASTIC)

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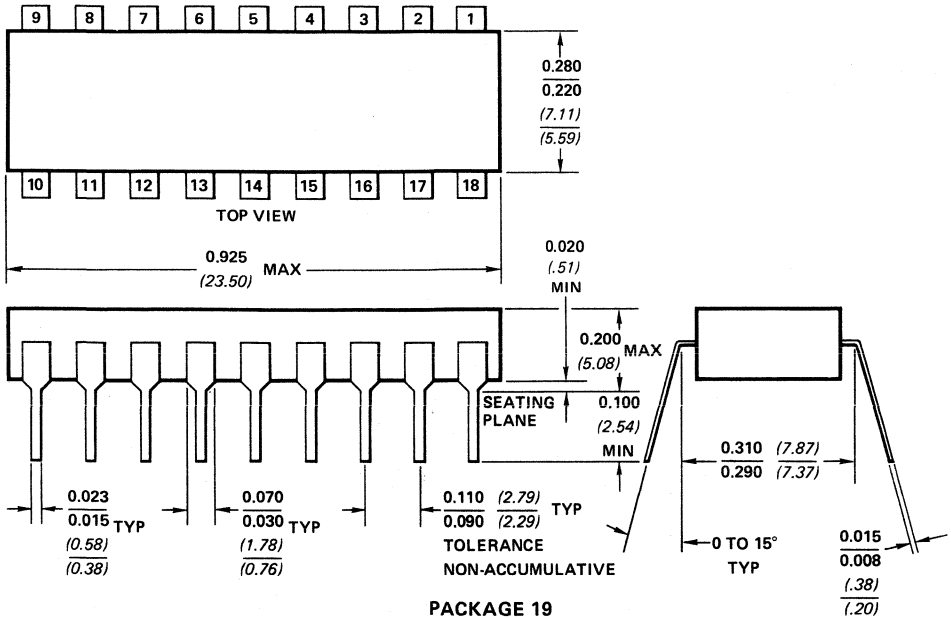

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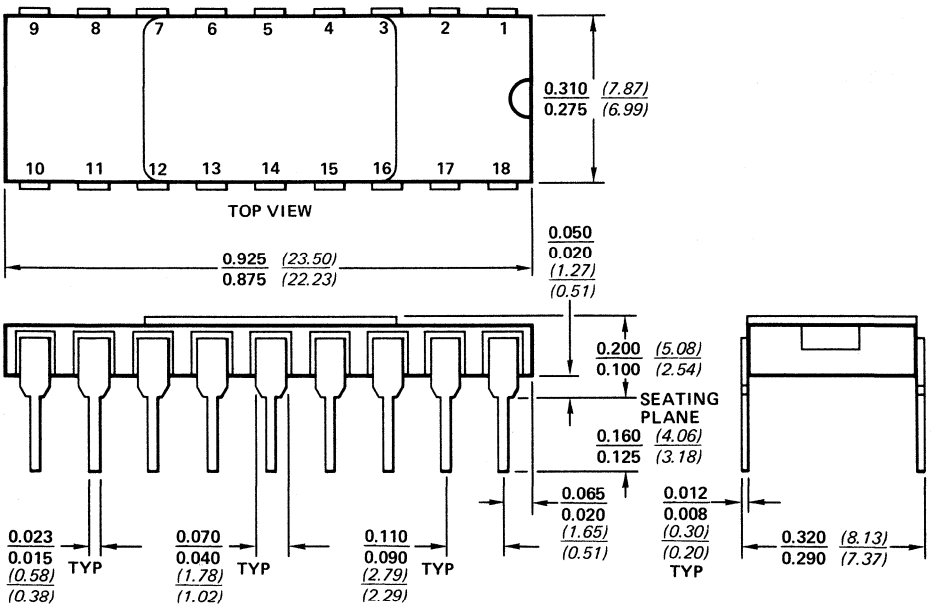

PACKAGE 20
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- NOTCH IN END OF PACKAGE VISIBLE FROM TOP AND/OR BOTTOM

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Waltham, MA 02154
(617)890-7180
Twx: 710-324-1783

Central

Siliconix incorporated
1040 S. Milwaukee, Suite 117
Wheeling, IL 60090
(312)541-0131
Twx: 910-576-2778

Siliconix incorporated
4615 W. Streetsboro Rd.
Richfield, OH 44286
(216)659-9305
Twx: 810-427-2978

Northwestern

Siliconix incorporated
2201 Laurelwood Rd.
Santa Clara, CA 95054
(408)988-8000
Twx: 910-338-0227

Southwestern

Siliconix incorporated
1525 E. 17th St., Suite L
Santa Ana, CA 92701
(714)547-4474
Twx: 910-595-2643

Sales Representatives

ALABAMA, Huntsville (35803)
Rep. Inc.
11527 S. Memorial Pkwy.
(205)881-9270
Twx: 810-726-2102

ARIZONA, Phoenix (85034)
Quatra Incorporated
2430 South 20th Street
(602)252-5885
Twx: 910-951-1369

CALIFORNIA, Cupertino (95014)
Costar Incorporated
10080 North Wolfe Rd., Suite SW3-175
(408)446-9339
Twx: 910-338-0206

CALIFORNIA, Irvine (92714)
Celtec Company
18009 Sky Park Cr., Suite B
(714)557-5021
Twx: 910-595-2512

CALIFORNIA, San Diego (92111)
Celtec Company
7867 Convoy Ct., Suite 312
(714)279-7961
Twx: 910-335-1512

CALIFORNIA, Sherman Oaks (91403)
Celtec Company
15335 Morrison Street
Suite 215
(213)783-0620
Twx: 910-495-2008

COLORADO, Littleton (80122)
Quatra Incorporated
2275 E. Arapahoe Road, Suite 217
(303)795-3187
Twx: 910-935-0874

CONNECTICUT, Ridgefield (06877)
Phoenix Sales Company
389 Main Street
(203)438-9644
Twx. 710-467-0662

FLORIDA, Ft. Lauderdale (33318)
Perrott Associates
P. O. Box 15067
(305)792-2211
Twx: 510-955-9831

FLORIDA, Largo (33540)
Perrott Associates
511 Rosery Rd. NE
(813)585-3327
Twx: 810-866-0328

FLORIDA, Orlando (32807)
Perrott Associates
1607 Forsyth Road
(305)275-1132
Twx: 810-850-0103

GEORGIA, Tucker (30084)
Rep. Inc.
1944 Cooledge Road
(404)938-4358

ILLINOIS, Northfield (60093)
Electron Marketing Corp.
500 Central Ave.
(312)441-7477
Twx: 910-992-0686

INDIANA, Carmel (46032)
Rich Electronic Marketing
599 Industrial Dr.
(317)844-8462
Twx: 810-260-2631

INDIANA, Fort Wayne (46804)
Rich Electronic Marketing
3448 W. Taylor St.
(219)432-5553
Twx: 810-332-1404

KANSAS, Shawnee Mission (66212)
BC Electronics
P. O. Box 12485
(913)888-6680
Twx: 910-749-6414

KANSAS, Wichita (67207)
BC Electronics
6405 E. Kellogg, Suite 14
(316)684-0051

MARYLAND, Baltimore (21227)
Coulbourn DeGreif, Inc.
5205 East Drive
(301)247-4646
Twx: 710-236-9011

MASSACHUSETTS, Reading (01867)
Kanan Associates
100 Main Street
(617)944-8484
Twx: 710-393-6552

MICHIGAN, Bloomfield Hills (48013)
Enco Marketing Inc.
860 West Long Lake Road
(313)642-0203
Twx: 810-232-1669

MINNESOTA, Minneapolis (55435)
KELCOM
5200 West 73rd Street
(612)835-0242
Twx: 910-576-2740

MISSOURI, Hazelwood (63042)
BC Electronics
300 Brookes Dr., Suite 206
(314)731-1255
Twx: 910-762-0600

NEW YORK, Syracuse (13206)
T² Electronics
4054 New Court Ave.
(315)463-8592
Twx: 710-541-0554

NEW YORK, Victor (14564)
T² Electronics
2 E. Main St.
(716)924-9101
Twx: 510-254-8542

NORTH CAROLINA, Cary (27511)
Montgomery Marketing
P.O.B. 520, 1212 Lane Dr.
(919)467-6319
Twx: 510-920-0634

OHIO, Dayton (45414)
Lyons Corporation
4812 Frederick, Suite 101
(513)278-0714

OHIO, Highland Heights (44143)
Lyons Corporation
6151 Wilson Mill Rd., Suite 101
(216)461-8288

PENNSYLVANIA, Erdenheim (19118)
GCM Associates
1014 Bethlehem Place
(215)233-4600
Twx: 510-661-9170

TENNESSEE, Jefferson City (37760)
Rep. Inc.
P.O.B. 287
(615)475-4105
Twx: 810-570-4203

TEXAS, Houston (77022)
Semiconductor Sales Associates
4101 N. Freeway, Suite 202
(713)661-0681

TEXAS, Richardson (75080)
Semiconductor Sales Associates
P.O. Box 2618
(214)231-6181

VIRGINIA, Charlottesville (22901)
Coulbourn DeGreif, Inc.
1616 Inglewood Dr.
(804)977-0031
Twx: 710-236-9011

WASHINGTON, Seattle (98107)
Blair Hirsh Co.
4013 Leary Way NW
(206)783-3423

WISCONSIN, Milwaukee (53220)
JM Sales
6522 W. Forest Home Ave.
(414)546 0040
Twx: 910-576-2778

Canada

ONTARIO, Etobicoke (M9C 1E7)
R.F.Q. Ltd.
385 The West Mall, Suite 209
(416)626-1445
Twx: 610-492-2540

QUEBEC, (H9G 2H8)
R.F.Q. Ltd.
P.O. Box 213, Dollard Des Ormeaux
(514)694-5724
Tix: 05821762

U.S. Chip Distributor

FLORIDA, ORLANDO (32807)
Chip Supply Inc.
1607 Forsyth Road
(305) 275-3810
Tlx: 810-850-0103

3

Siliconix

International Sales Offices

European Sales Offices

FRANCE
Siliconix S.A.R.L.
70-72 Avenue du General de Gaulle
Echat 660
94022 Creteil Cedex
Tel: 377.12.51
Tlx: Silconx 230389F

WEST GERMANY
Siliconix GmbH
Postfach 1340
Johannesstrasse 27
D-7024 Filderstadt-1
Tel: (0711)702066
Tlx: 7-255 553

UNITED KINGDOM
Siliconix Ltd.
Brook House
Northbrook Street
Newbury, Berks
RG13 1AH
Tel: (0635)64846
Tlx: 849357

Siliconix Ltd.
Morriston, Swansea
United Kingdom SA6 6NE
Tel: (0792)74681
Tlx: 48197

Far East Sales Offices

HONG KONG
Siliconix (H. K.) Ltd.
5/6/7th Floors
Liven House
61-63 King Yip Street, Kwun Tong
Kowloon, Hong Kong
Tel: 3-427 151
Tlx: 74449 SILX HX

JAPAN
Siliconix DISC Japan Branch
101 Daigo Tanaka Bldg.
4-4 Iidabashi, 3-Chome
Chiyoda-Ku, Tokyo, Japan 102
Tel: 03-262-4777
Tlx: J23411

TAIWAN
Siliconix (Taiwan) Ltd.
Nantze Export Processing Zone
Kaohsiung
Tel: 362010, 362019
Tlx: 785 712 35

European Distributors/Representatives

AUSTRIA
Ing. Ernst Steiner
A-1130 Wien
Geylinggasse 16
Tel: 222/822674
Tlx: 135026

BELGIUM
Ritro Electronics BV
172 Plantin en Moretuslei
B-2000 Antwerpen-B
Tel: 031-353272
Tlx: 33637

DENMARK
Ditz Schweitzer A.S.
Vallensbaekvej 41
DK-2600 Glostrup
Tel: (01)45-30-44
Tlx: 33257

FINLAND
Oy Findip AB
Teollisuustie 7. P.O.B. 34
SF 02700 Kauniainen
Tel: 90-502255
Tlx: 12-3129

FRANCE
Almex
48 Rue de L' Aubepine
92160 Antony
Tel: 666-21-12
Tlx. 250067

Alrodis
40 Rue Villon
69008 Lyon
Tel: (78) 695952
Tlx: 330174

Aquitaine Composants
30 Rue Denfert Rochereau
33400 Talence
Tel: (56) 80 24 70

A. Baltzinger
18-26 Route du General de Gaulle
67300 Schiltigheim
Tel: (88) 331852
Tlx: 870952F

Ouest Composants
5 rue Lesage
3500 Rennes
Tel: (99) 360058
Tlx: 730004

Sanelec Electronique
7 Rue de la Couture
Z 1, de la Pilaterie
59700 Marcq-en-Baroeuil
Tel: (20) 98-92-13
Tlx: 160 143F

SCAIB
80 Rue d'Arceuil
Z Silic 137
Rungis, 94523 Cedex
Tel: 687-23-13
Tlx: 204 674F

GERMANY
Ditronic GmbH
IM Asemwald 48
7000 Stuttgart 70
Tel: (0711) 724844
Tlx: 07-255638

Ing. Buro K.H. Dreyer
Flensburger Strasse 3
2380 Schleswig
Tel: (04621) 23121
Tlx: 02-21334

EBV Elektronik GmbH
Gabriel-Max Strasse 72
8000 München 90
Tel: (089) 644055
Tlx: 05-24535

EBV Elektronik GmbH
Alexanderstrasse 42
7000 Stuttgart 1
Tel: (0711) 247481
Tlx: 07-22271

EBV Elektronik GmbH
Ostrasse 129
4000 Dusseldorf
Tel: (0211) 84846/7
Tlx: 08-587267

EBV Elektronik GmbH
In der Meineworth 9A
3006 Burgwedel 1/Hannover
Tel: (05139) 4570
Tlx: 09-23894

EBV Elektronik GmbH
Myliusstrasse 54
6000 Frankfurt 1
Tel: 0611/7204 16/7
Tlx: 04-13590

iv-electronic
Klaus Vespermann Kg
Bachstrasse 30a
6380 Bad Homburg V.D.H.
Tel: (06172) 23061-5
Tlx: 0415864

Ultratronik GmbH
Munchner Strasse 6
8031 Oberaltting-Seefeld
Tel: (08152) 7774
Tlx: 05-27832

Unitronic Schluter GmbH u. Co. KG
Manskestrasse 29
3160 Lerthe
Tel: (05132) 53001
Tlx: 09-22084

GREECE
General Electronics, Ltd.
209 Thevon St.
Nikaia, Piraeus 77
Tel: 361-8145
Tlx: 212949 GELT GR

HOLLAND
Datron B.V.
P.O. Box 75
1243ZH S.Graveland-NL
Tel: 035-60834
Tlx: 4 3943

Ritro Electronics BV
Gelreweg 22
Postbox 123
3770 AC Barneveld-NL
Tel: 03420-5041
Tlx: 40553

ITALY
Adelsy
Via Domenichino 12
20149 Milano
Tel: (02) 4985051
Tlx: 33 2423

Dott. Ing. Giuseppe DeMico
Via Manzoni 31
20121 Milano
Tel: 653131
Tlx: (02) 312035

NORWAY
A. S. Kjell Bakke
Postbox 143
2010 Strommen, Nygaton 48
Tel: (02) 71 18 72 71 53 50
Tlx: 19407

SPAIN
ATAIO
Enrique Larreta 10Y12
Madrid 16
Tel: 733.05.62 or 733.37.00
Tlx: 27249

SWEDEN
Komponentbolaget NAXAB
Box 4115
S-17104 Solna
Tel: 08.985140
Tlx: 17912 KOMP

SWITZERLAND
Kontron Electronic AG
Bernerstrasse Sud 169
8048 Zurich
Tel: 01-62-82-82
Tlx: 58836

UNITED KINGDOM
Dage Eurosem Ltd.
Haywood House
High Street
Pinner
MIDDLESEX
Tel: 01-868-0028
Tlx: 24506

Linburg Electronics Ltd.
Hillend Industrial Estate
Dunfermline
SCOTLAND
Tel: (0383) 823222
Tlx: 727438

Macro-Marketing Ltd.
396 Bath Road
Slough, Berk
Tel: (06286) 4422
Tlx: 847945

Semiconductor Specialists (UK) Ltd.
Premier House, Fairfield Road
Yiewsley, West Drayton
MIDDLESEX
Tel: (08954) 45522
Tlx: 21958

Woolley Components Ltd.
Tudor Road, Broadheath Ind. Est.
Altrincham, CHESHIRE WA145RZ
Tel: (061941) 1911
Tlx: 669735

YUGOSLAVIA
Belram S.A.
83 Avenue des Mimosas
1150 Brussels, Belgium
Tel: 734.33.32 734.26.19
Tlx: 21790

Other International Distributors/Representatives

ARGENTINA
Corte & Cia, S.R.L.
San Juan 1301
Buenos Aires
Tel: 27-0101
Tlx: 012-1992

EMSE Electronica S.A.
Div. Semiconductores
Ayacucho No. 311
1025 Buenos Aires
Tel: 40-2071

AUSTRALIA
STC Cannon Components PTY. LTD.
248 Wickham Road - P.O. Box 62
Moorabbin, Victoria 3189, Australia
Tel: Melbourne 95-1566
Tlx: Melbourne AA 30877
Cable: CANNONLEC - MELBOURNE

BRAZIL
Cosele LTDA
Rua da Consolacao,
867-Cj 22
01310 Sao Paulo
Tel: 257-3535 or 258-4325
Tlx: 1130869-CSEL-BR

INDIA
Zenith Electronics
541 Panchratna
Mama Parmanand Marg
Bombay 400004
Tel: 384214
Tlx: 011-3152

ISRAEL
Talviton Electronics, Ltd.
9 Biltmore St.
Tel Aviv
Tel: 44.45.72
Tlx: Vitko 33400

JAPAN
Teijin Advanced Products Corp.
1-1 Uchisawai-cho, 2-Chrome
Chiyoda-Ku, Tokyo, 100
Tel: (03) 506-4670
Tlx: J-23548

KOREA
Yeonil & Co. Ltd.
KPO Box 1112
Seoul
Tel: 65-0461
Tlx: K24123

MEXICO
Mexel
Tlacoquemecatl No. 139-401
Mexico 12, D.F.
Tel: 575-78-68, y 575-79-24
Tlx: MEXEL 0177 3197

NEW ZEALAND
Electronic Component Services
Div. of Airspares NZ Ltd.
P. O. B. 1048, Palmerston North
Tel: 77-407
Tlx: NZ3766

SOUTH AFRICA
Electrolink (Pty) Ltd.
P.O. Box 1020
Capetown
Tel: 457656/7
Tlx: 57-7320

TAIWAN
Don Business Corp.
No. 265 Chang Chung Rd.
Taipei
Tel: 571-2911
Cable: "DONBC" TAIPEI
Tlx: 25641 DONBC

VENEZUELA
IBARS & Cia, S.A.
Centro Ciudad Commercial Tamanaco
Nivel C2, Local 53-C-03
Chuao-Caracas
Apartado 68493
Caracas 106
Tel: 928053
Tlx: 21795 Teletipos a/c IBARS
Cables: IBARS-CARACAS